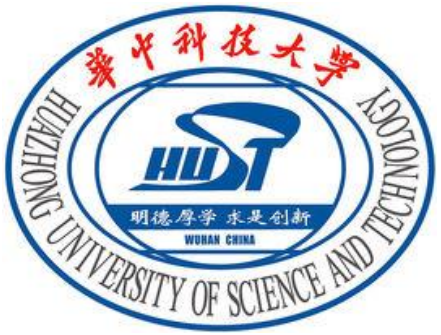
DREAM: Data Representation Aware of Damage to Extend the Lifetime of MLC NAND Flash Memory

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Xubin He

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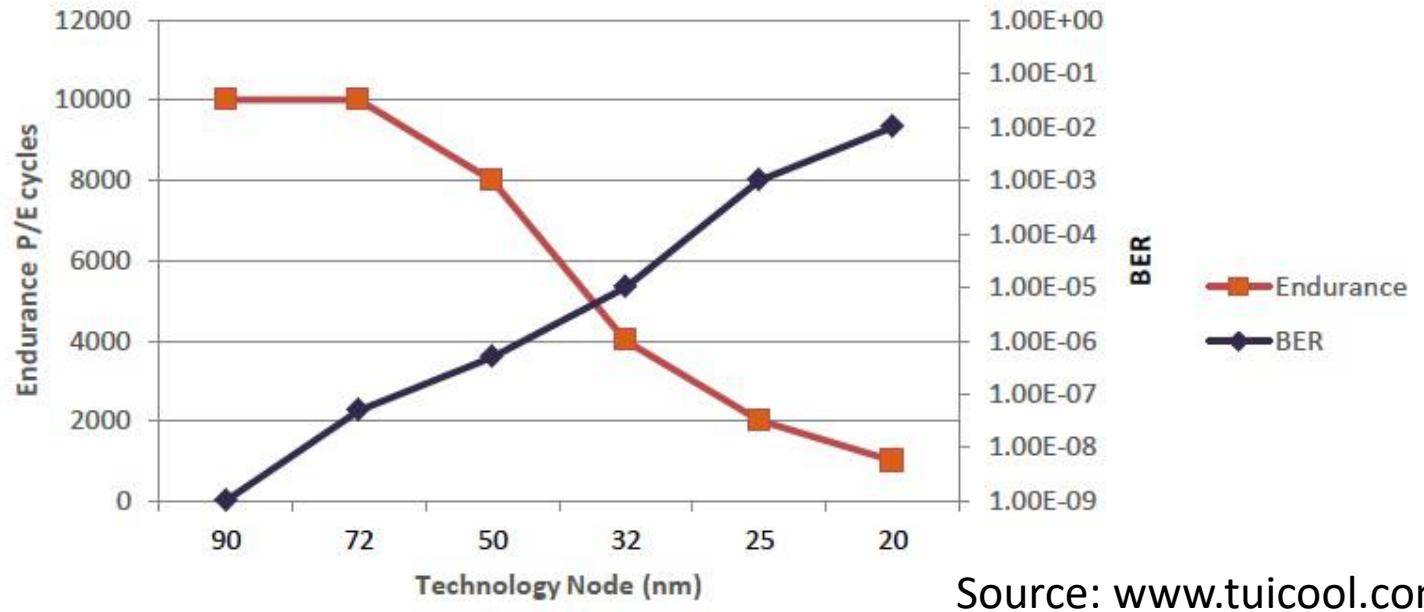


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Boston, MA, USA, July 09-10, 2018

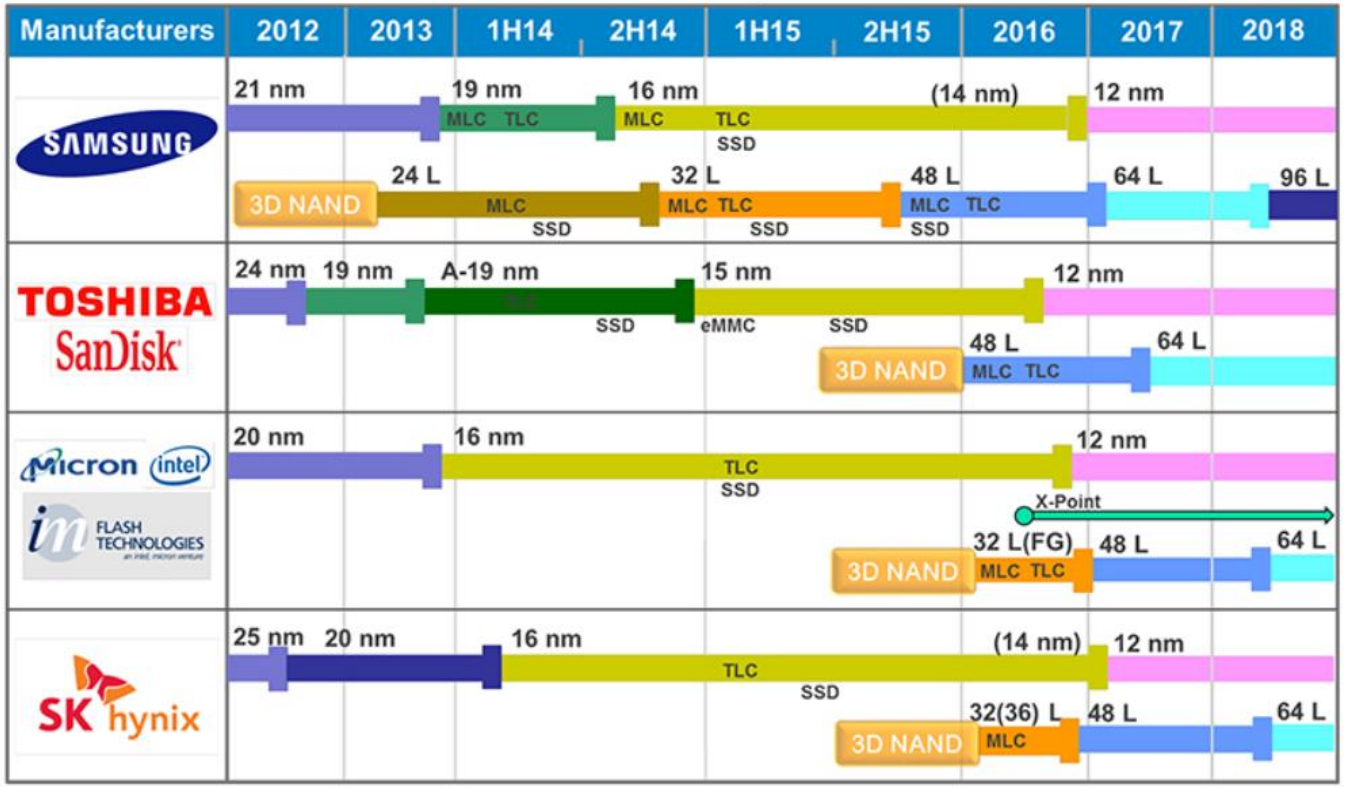
Outline

- Motivation
- Background and related work
- DREAM design
- Evaluation
- Conclusions

NAND Flash Memory



Source: www.tuicool.com



$/GB:

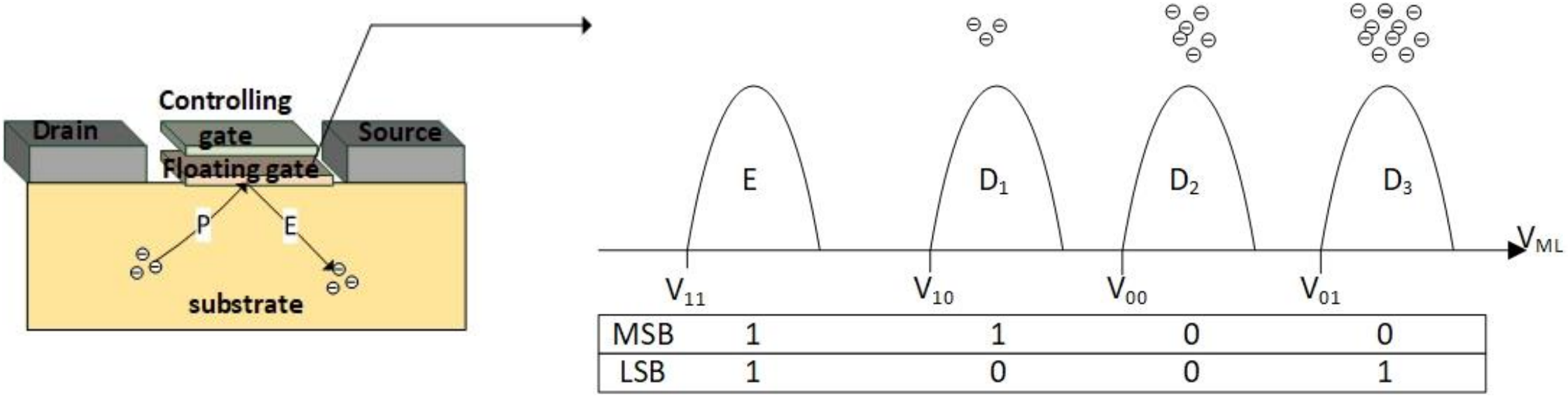


lifetime:



Source: http://www.techinsights.com

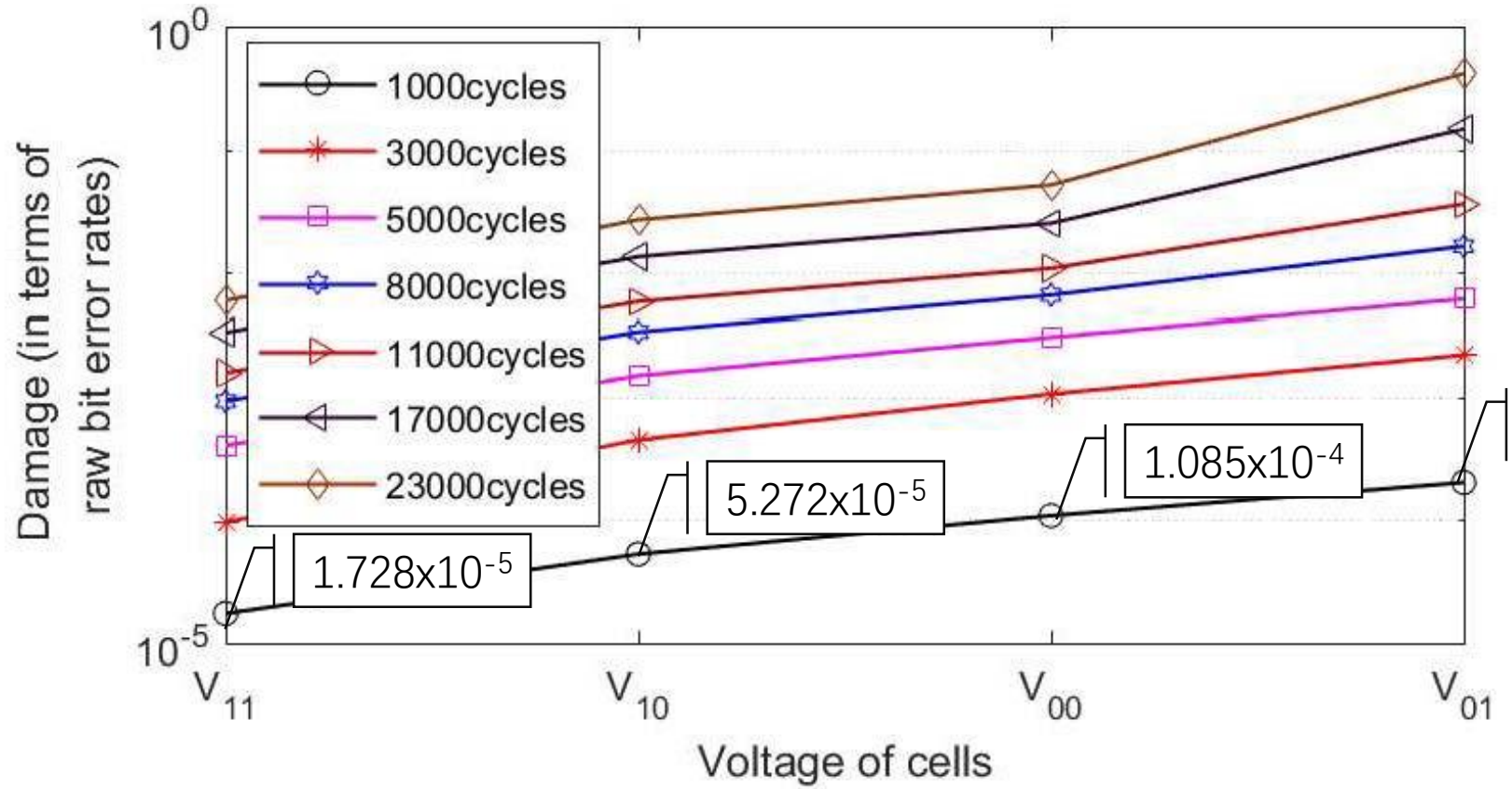
MLC NAND flash memory cell



MSB	1	1	0	0
LSB	1	0	0	1

- The P/E operations can significantly damage the oxide layer.
- **MLC NAND Flash memory cells suffer content-dependent memory damage.**

Damage of different voltages



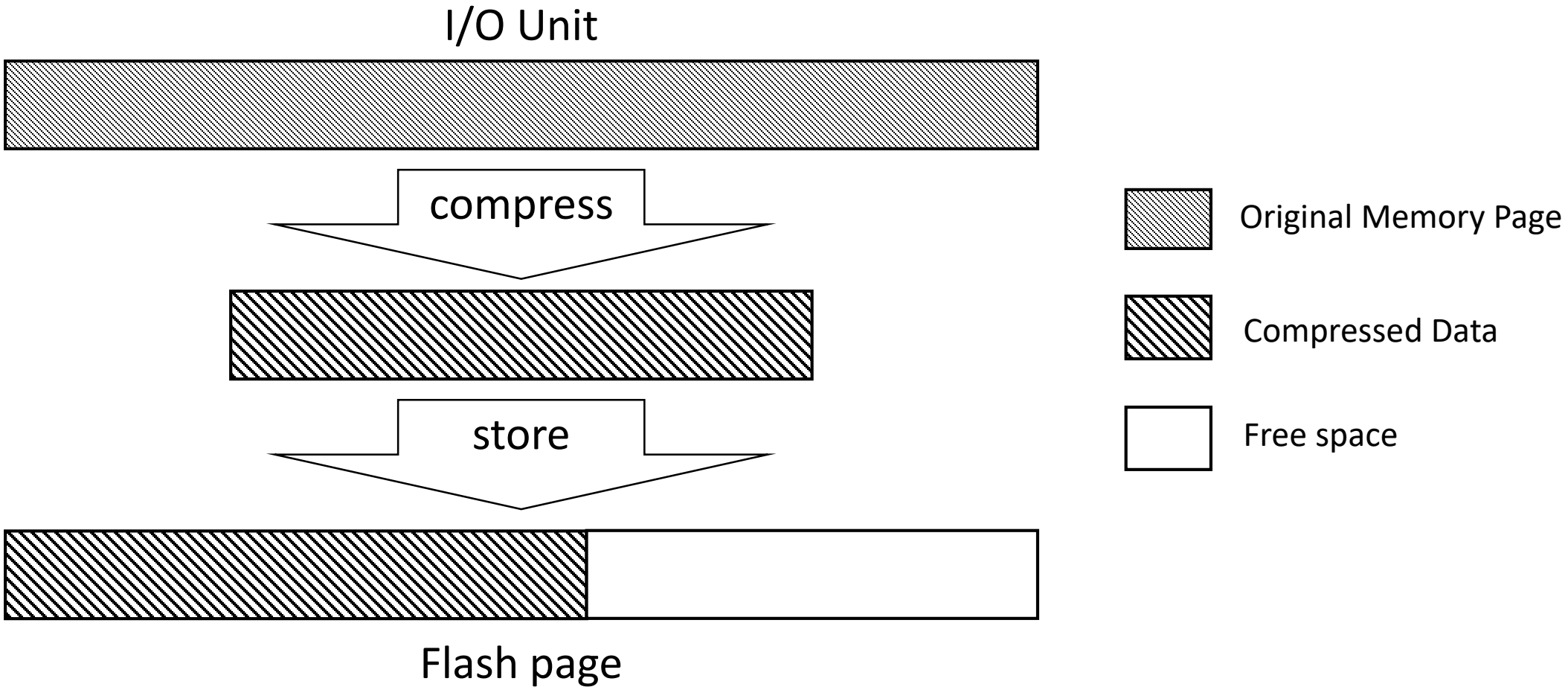
Average damage:
$(1.728\text{x}10^{-5} + 5.272\text{x}10^{-5} + 1.085\text{x}10^{-4} + 2.021\text{x}10^{-4})/4$
$= 9.515\text{x}10^{-5}$

V_{01} contributes:
$$\frac{25\% \times 2.021\text{x}10-4}{9.515\text{x}10-5} = 53.1\%$$

- **The damage increases exponentially with the growth of voltage**
  - Damage of different voltages: $V_{11} << V_{10} << V_{00} << V_{01}$

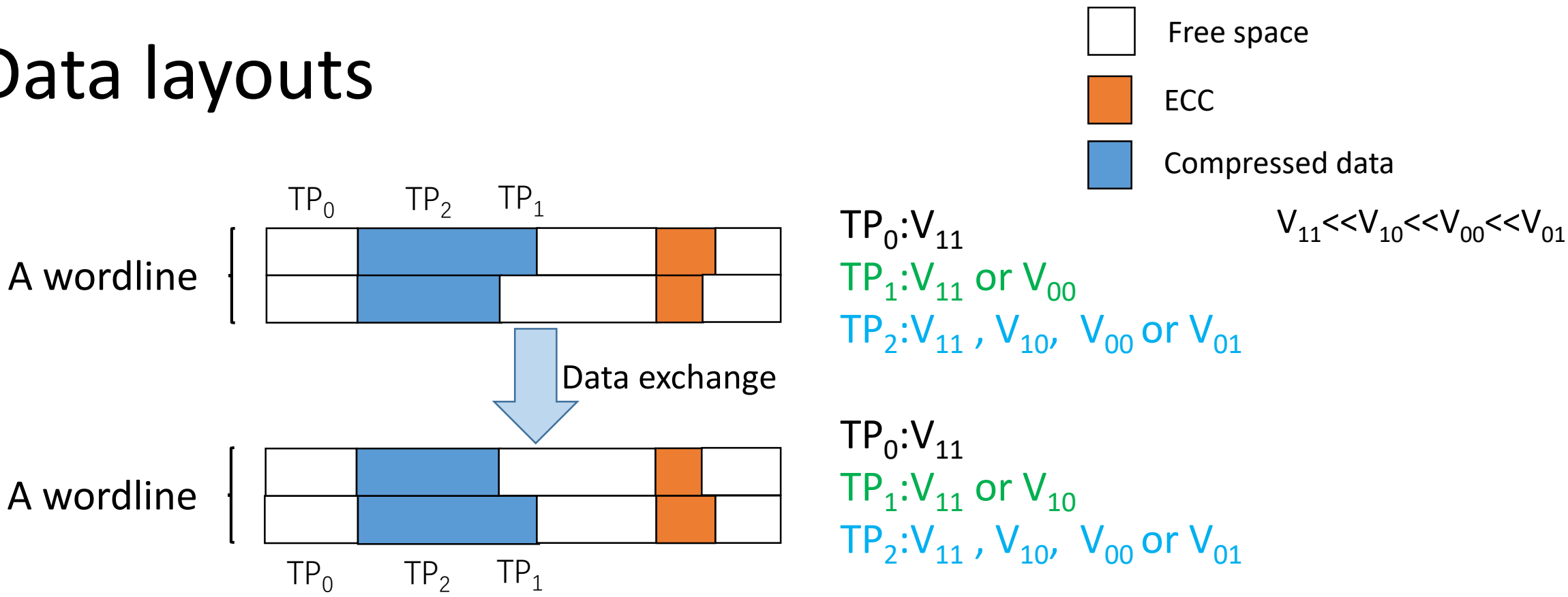
Data source: Jiangpeng Li, et al.(FAST'15)

Compression



Data compression ratio: *r* => Lifetime extends 1/r*?*

Data layouts



- One bit of the free space is only used to eliminate the usage of high voltages in one single cell.

Bits must be represented by the voltage of one single cell?

Our solution

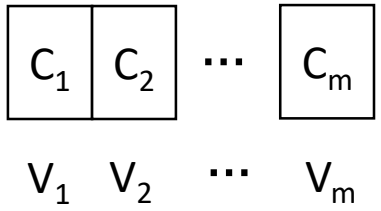
- Most of the damage is caused by high voltages.
  - If the usage of high voltages can be reduced, the average damage will be significantly reduced.
- Free space can be used to reduced the usage of high voltages.
  - Free space can be get by data compression or found in OOB space.
- Bits can be represented by voltage combinations of multiple cells.

Data Representation Aware of Damage (DREAM)

- Data representation
  - Using the voltage combinations of multiple cells instead of the voltage of one single cell to represent bits
  - Low-damage voltage combinations are used first.
- Data layout
  - Data is partitioned into zones
  - Additional metadata is stored in OOB space

DREAM

- Every *m* cells in a wordline form a group:(C_1;C_2; …;C_j; …;C_m)
- All the *m* voltages of a group denoted by an *m-tuple* (V_1;V_2; …;V_j; …;V_m)

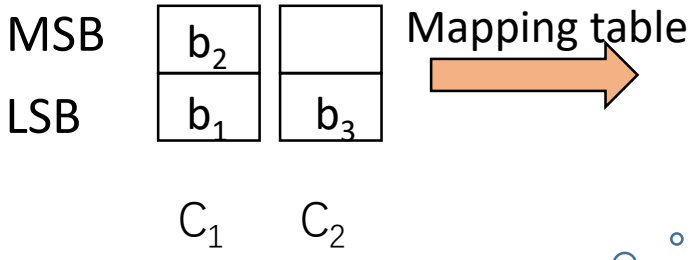


V_j:V_{11}, V_{10}, V_{00}, V_{01} (4 voltages)
m-tuple: 4^m voltage combinations

- Choosing the 2^i lowest damage voltage combinations to represent *i* bits. ($0 \leq i \leq 2m$)
- DREAM-m: m cells form a group

DREAM-2

$V_{11} << V_{10} << V_{00} << V_{01}$



#Bits / V_1 V_2	1	2	3	#Bits / V_1 V_2	1	2	3
V_{11} V_{11}	1	11	111	V_{10} V_{00}	-	-	000
V_{11} V_{10}	0	10	110	V_{10} V_{01}	-	-	001
V_{11} V_{01}	-	01	101	V_{10} V_{10}	-	-	010
V_{11} V_{00}	-	00	100	V_{10} V_{11}	-	-	011

V_{01} is used, but there is free space left

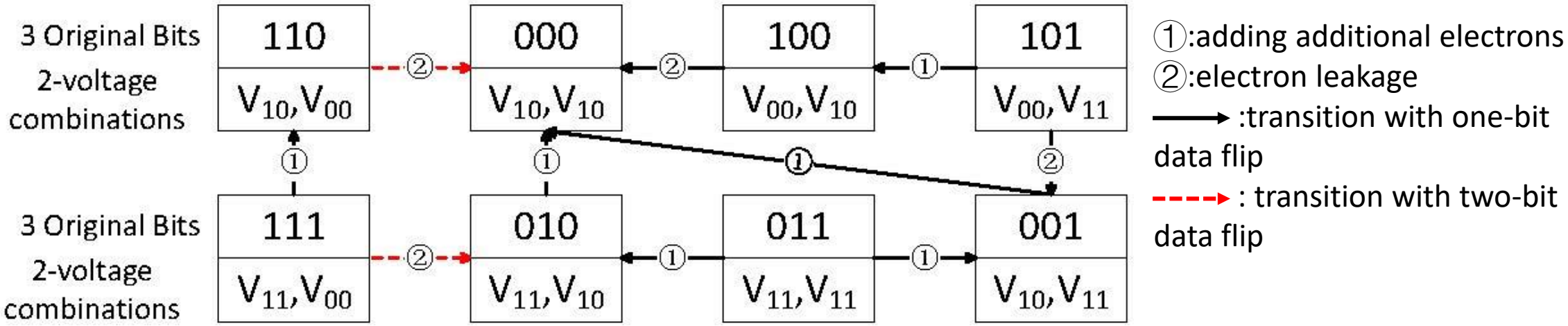
DREAM-2

#Bits / V_1 V_2	1	2	3	#Bits / V_1 V_2	1	2	3
V_{11} V_{11}	1	11	011	V_{11} V_{00}	-	-	111
V_{11} V_{10}	0	10	010	V_{00} V_{11}	-	-	101
V_{10} V_{11}	-	01	001	V_{10} V_{00}	-	-	110
V_{10} V_{10}	-	00	000	V_{00} V_{10}	-	-	100

Lowest-damage voltage combinations are used.

Voltage state transitions

- To limit the amplification of bit errors



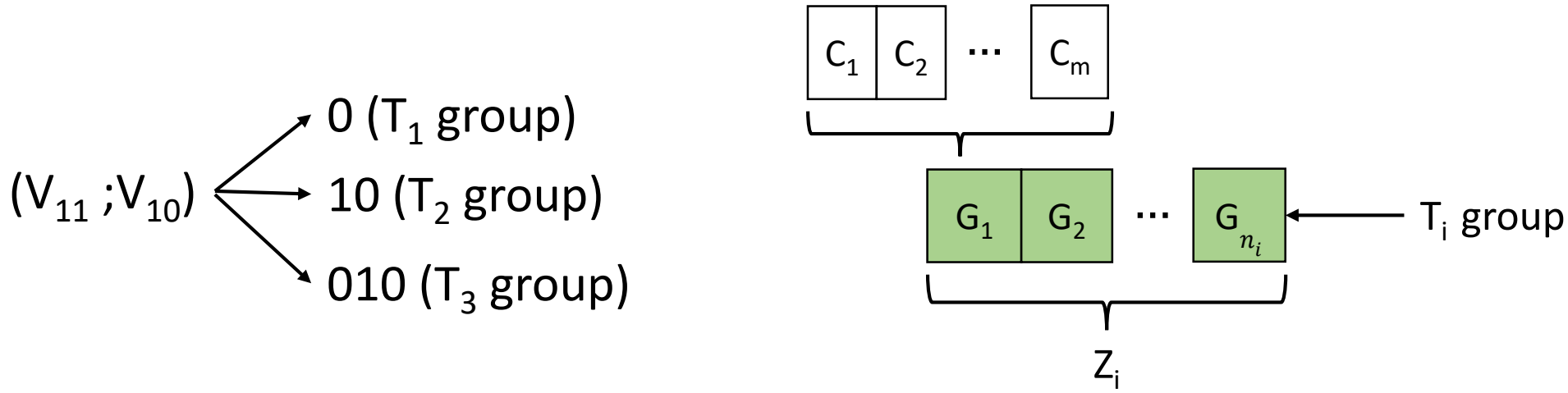
- 12 flipped bits after using DREAM v.s. 10 flipped bits under traditional representation

Additional metadata

A group can store i bits of data ($0 \leq i \leq 2m$)

T_i group: to store i bits in the cell group.

One certain voltage combination might represent different bits for different types of groups.



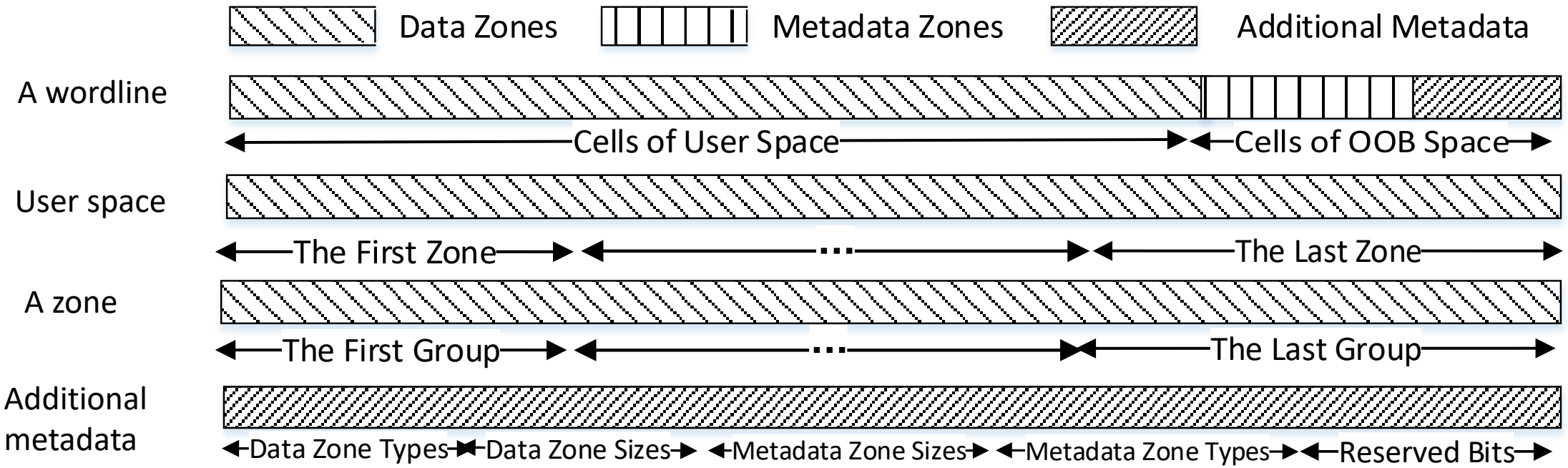
Zone: all the T_i groups are placed together to form zone Z_i

Additional metadata: to record the type and size of zones

Additional metadata

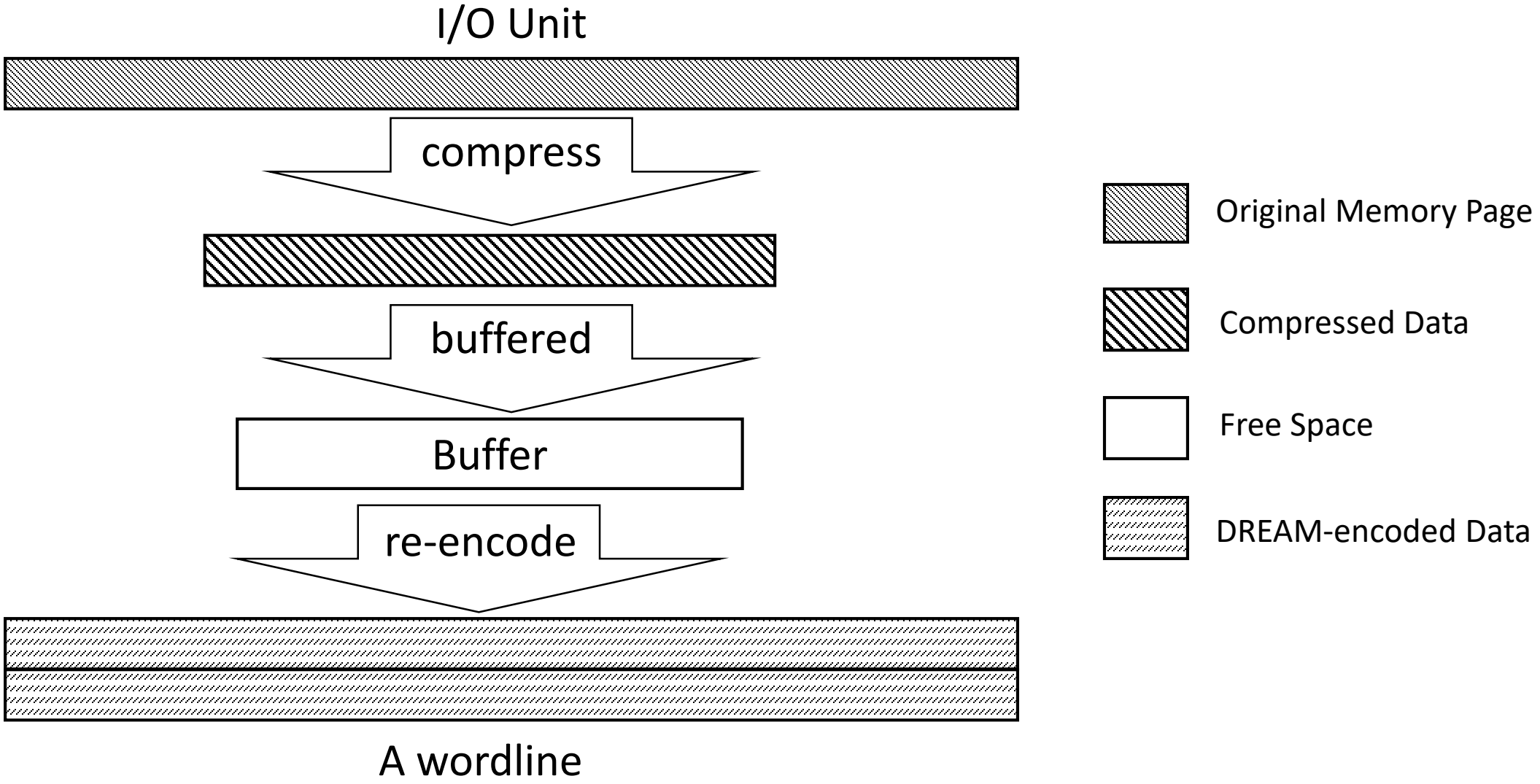
- Two constraints
  - The total capacity of all the zones should be large enough to store all the data.
  - The total cells in all the zones should not exceed the cells of user space in a wordline.
- A target
  - to minimize the total damage of a page
- simplex method

Data layout in a wordline

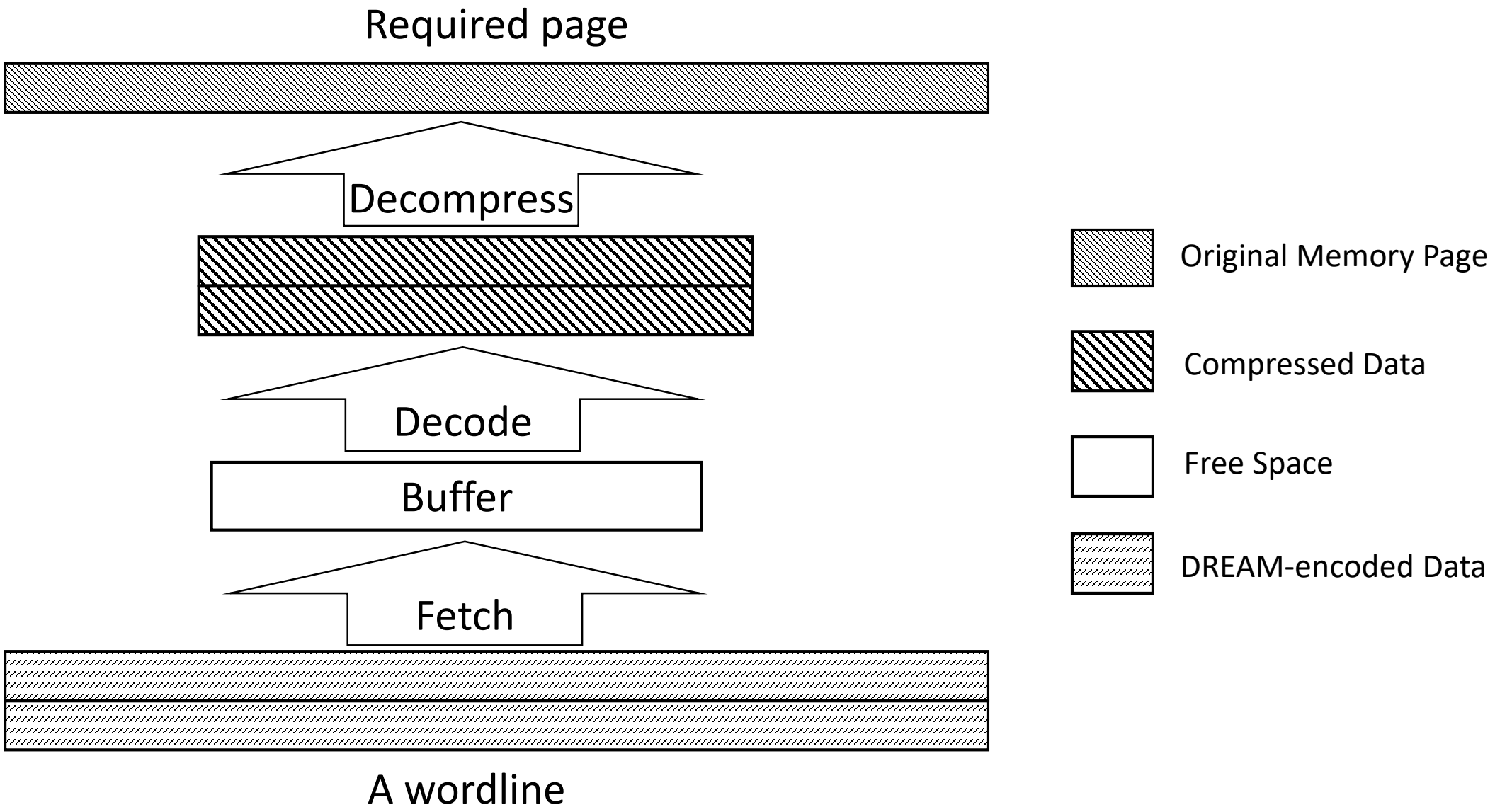


- DREAM is applicable to both the data and the metadata.
- Zone types and zone size depend on page size and data size

Write


I/O Unit
compress
buffered
Buffer
re-encode
A wordline
Original Memory Page
Compressed Data
Free Space
DREAM-encoded Data

Read


Required page
Decompress
Decode
Buffer
Fetch
A wordline
Original Memory Page
Compressed Data
Free Space
DREAM-encoded Data

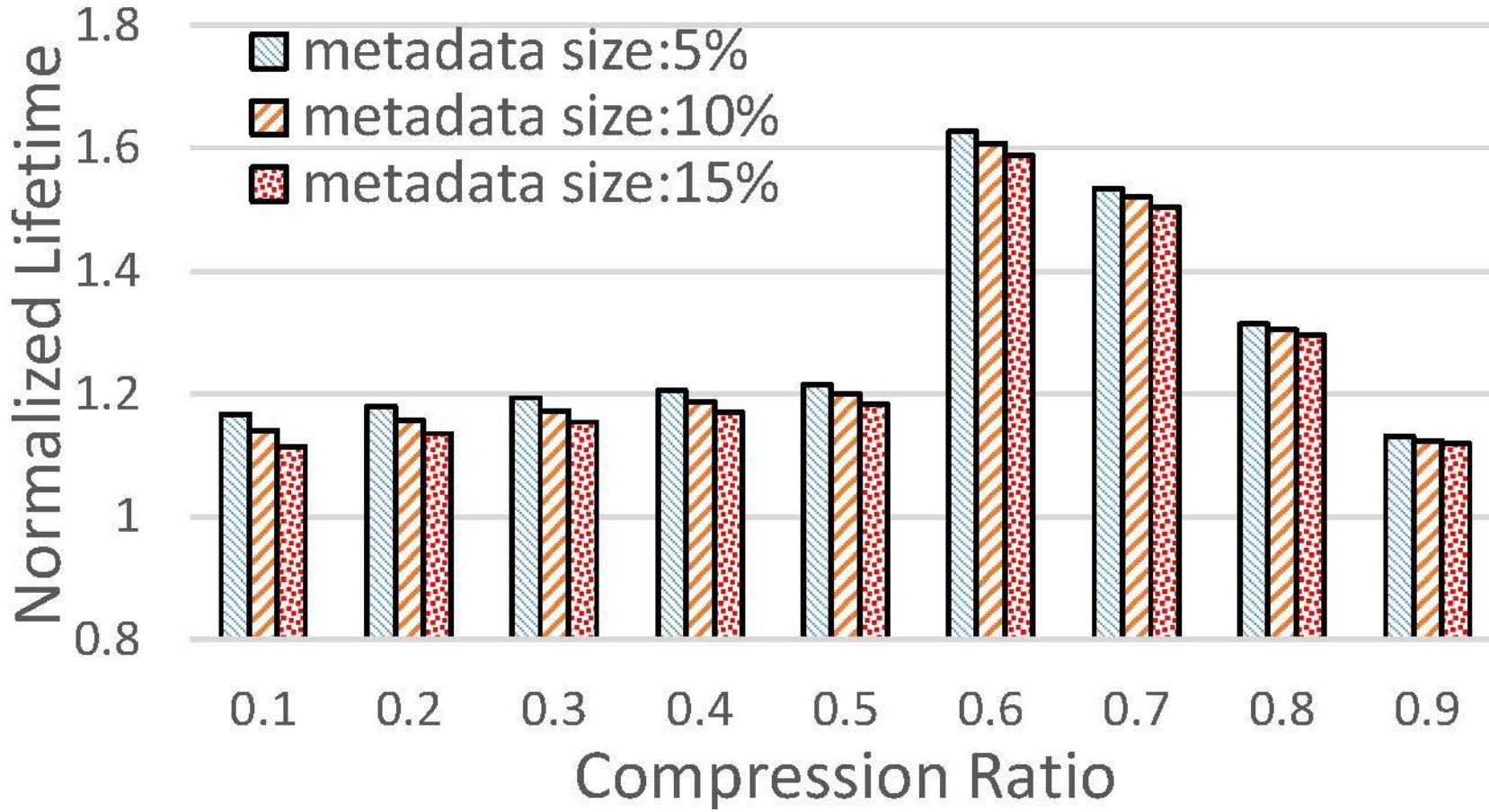
Evaluation

- Theoretical Analysis
  - Improvement of lifetime
- Simulation
  - Overall response time and throughput

Theoretical Analysis

- Lifetime: P/E cycles
- OOB space: 20% of the page size
- Compression ratio: ranges from 0.1 to 0.9
- Metadata size: ranges from 5% to 15% of the page size

Lifetime


metadata size:5%
metadata size:10%
metadata size:15%
Normalized Lifetime
1.8
1.6
1.4
1.2
1
0.8
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
Compression Ratio

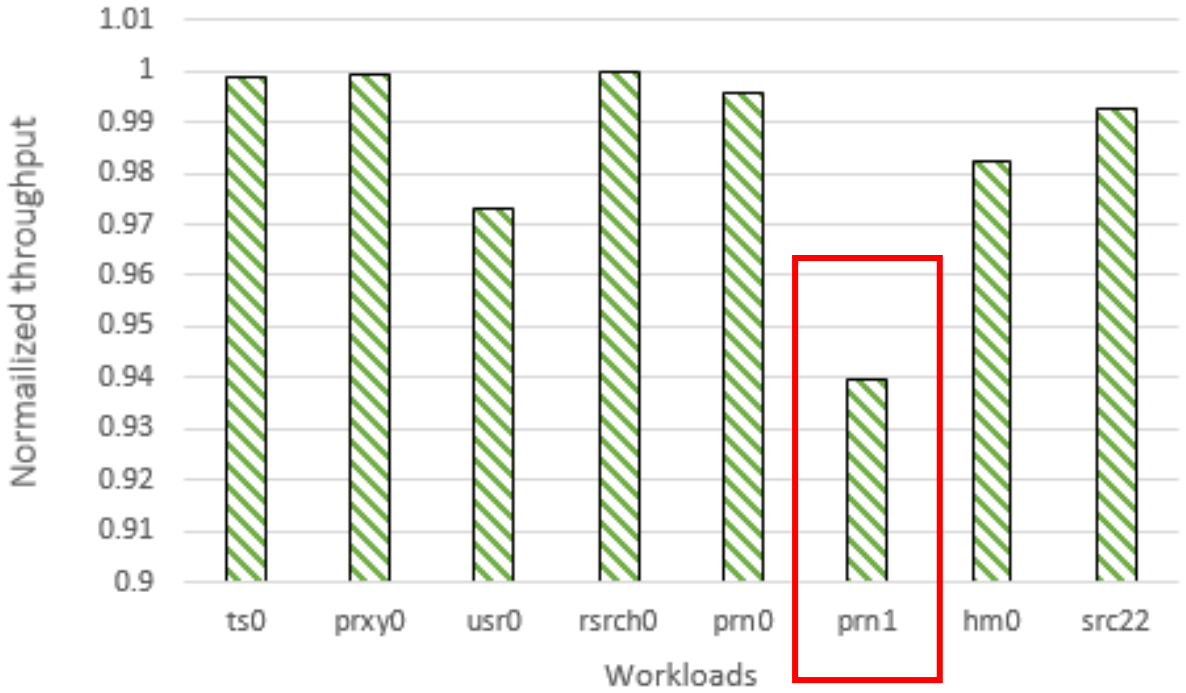
Simulations

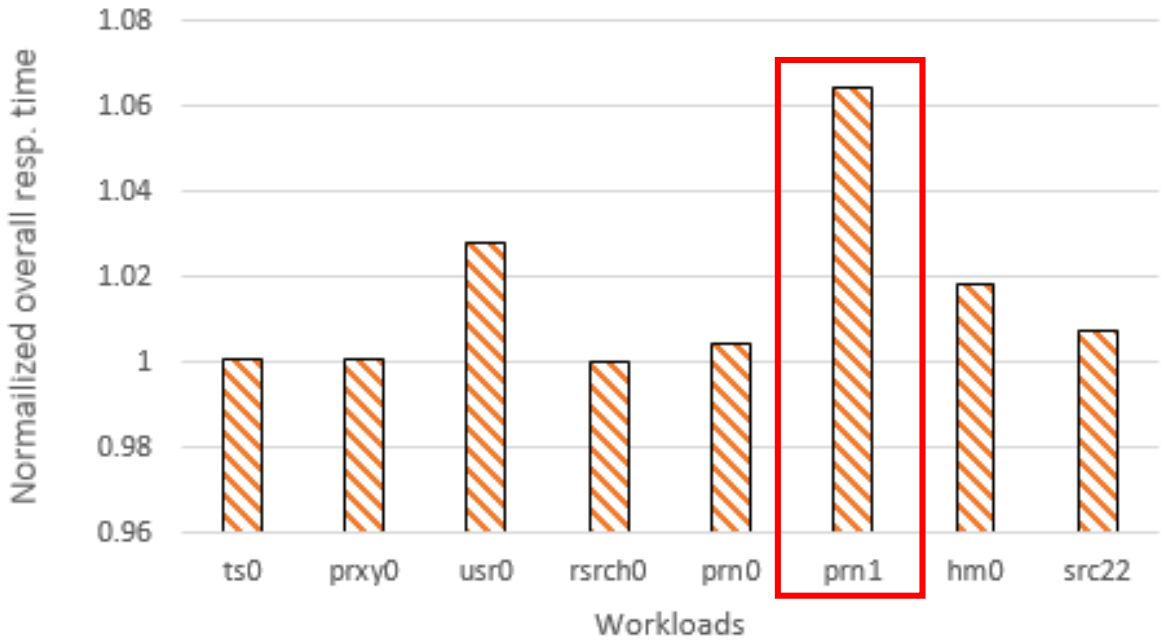
- Purpose
  - To evaluate the efficiency of DREAM
- Simulator
  - disksim-4.0 with ssdmodel

Traces	#R (M pages)	#W (M pages)	WR	ARS (KiB)	B (K)
ts0	0.5	2.0	0.79	9.0	4
prxy0	0.5	14.7	0.96	5.45	4
usr0	2.9	2.0	0.42	22.7	4
rsrch0	0.2	1.9	0.90	8.95	4
prn0	1.3	7.5	0.85	14.8	8
prn1	18.1	4.3	0.19	23.3	8
hm0	1.9	3.7	0.66	8.0	8
src22	1.7	3.1	0.65	56.3	8

R: Reads
W: Writes
WR: Write ratios
ARS:Average Request Sizes
B: Blocks per Plane

Simulation Results: Response time &Throughput





Conclusions

- We propose DREAM to extend the lifetime of MLC NAND Flash memory
  - Using the low-damage voltage combinations of multiple MLC cells instead of the voltage of one single MLC cell to represent bits
- We develop a theoretical model.
  - Extension of lifetime: over 25.8%
- Overhead is trivial and acceptable
  - Overall response time and throughput are affected by 1.5%

Thanks!

Questions?