Lifetime Improvement of NAND Flash-based Storage Systems *Using Dynamic Program and Erase Scaling*

Jaeyong Jeong*, Sangwook Shane Hahn*, Sungjin Lee†, and Jihong Kim*

** Seoul National University, Korea*

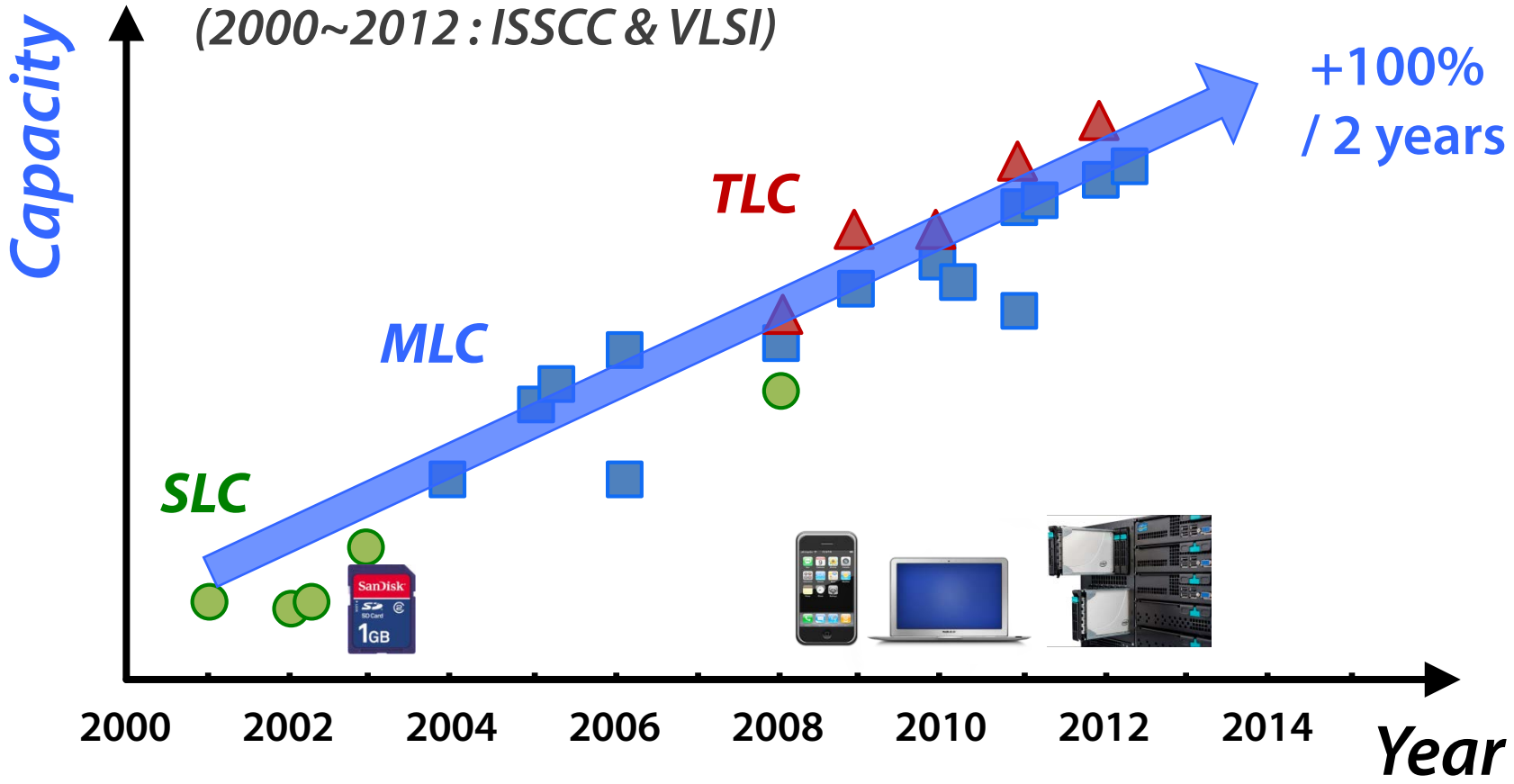
† Massachusetts Institute of Technology

12th USENIX Conference on File and Storage Technologies, 2014

Outline

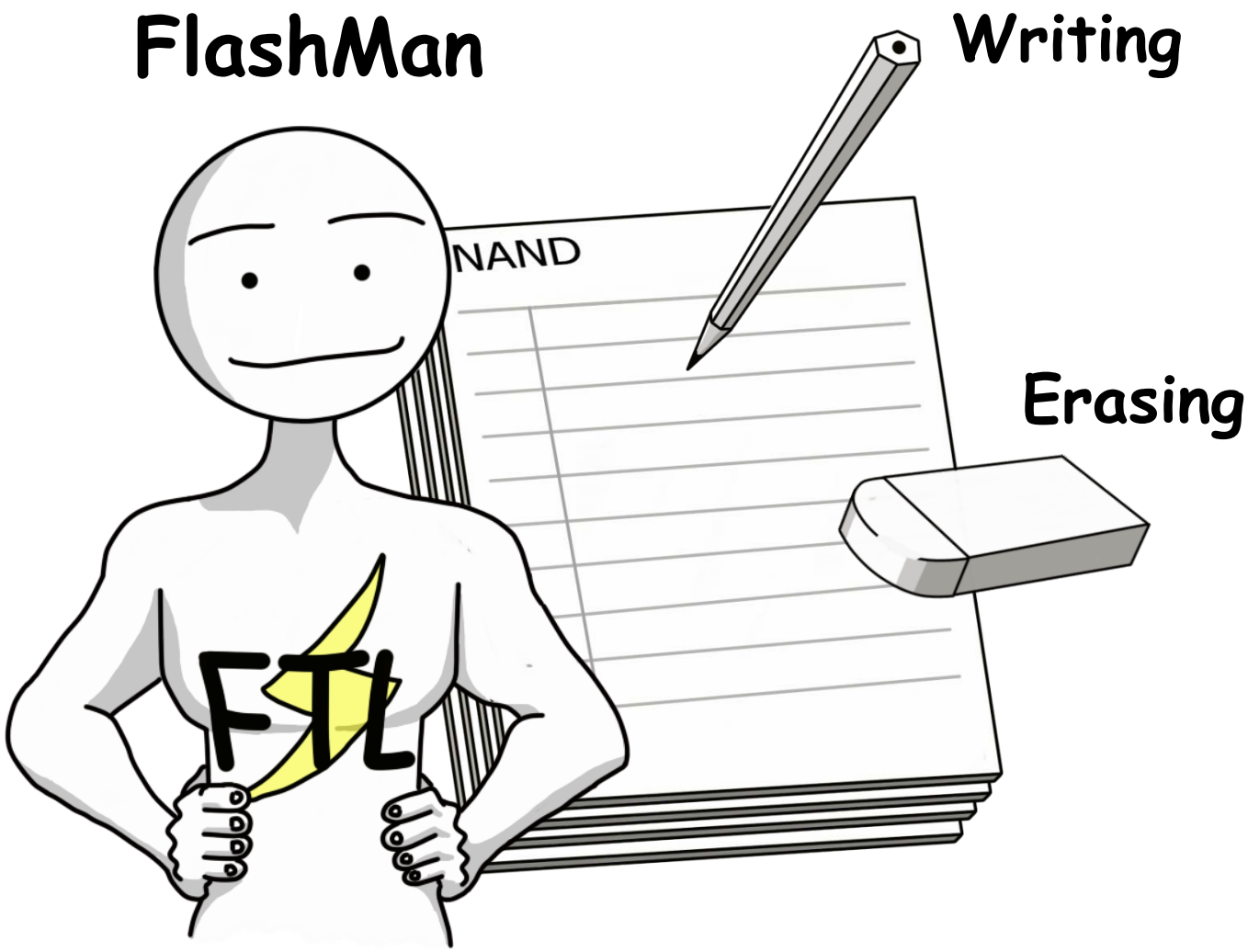
- **Lifetime Issues in NAND Flash-based Storages**
- Key Components of the DPES Approach
- Implementation of DPES-aware FTL
- Experimental Results
- Conclusions
- Q & A

Trend of NAND Device Technologies



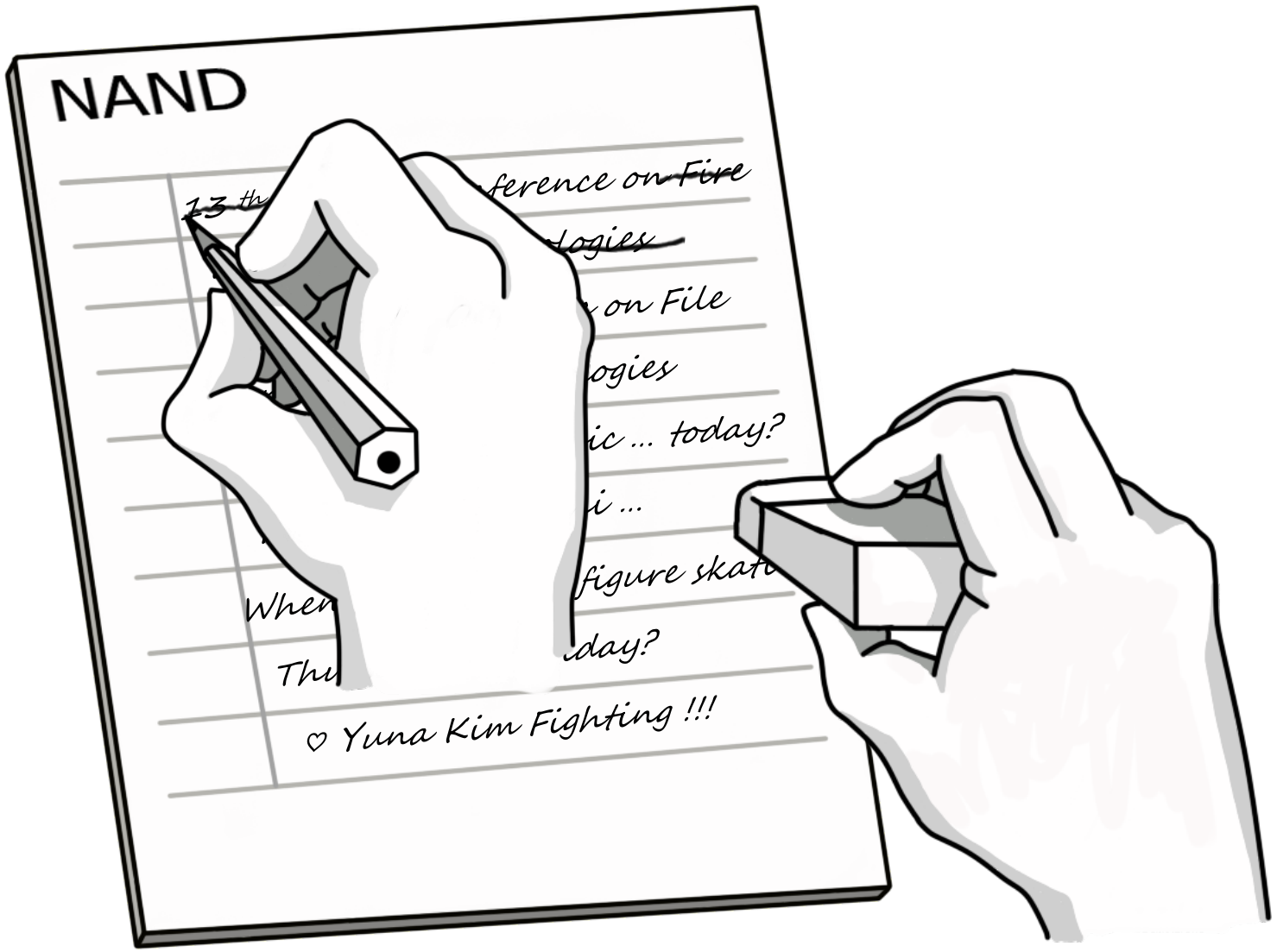
NAND capacity is continuously increased,
and NAND flash-based storages are widely adopted.

NAND Flash Memory is like Sheets of Paper

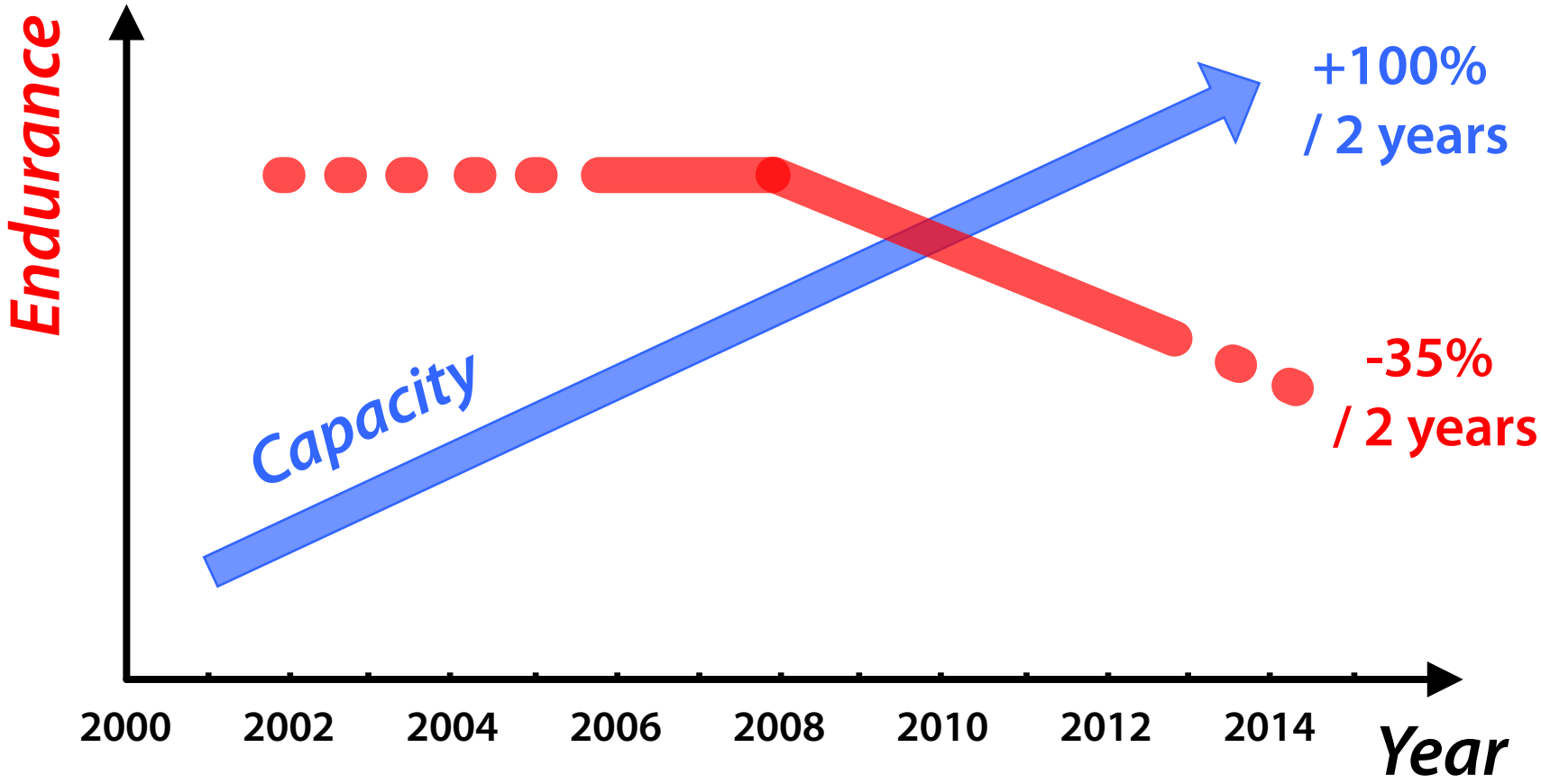


Illustrated by Jisung Park, Seoul National University

Writing Letters and Erasing Paper



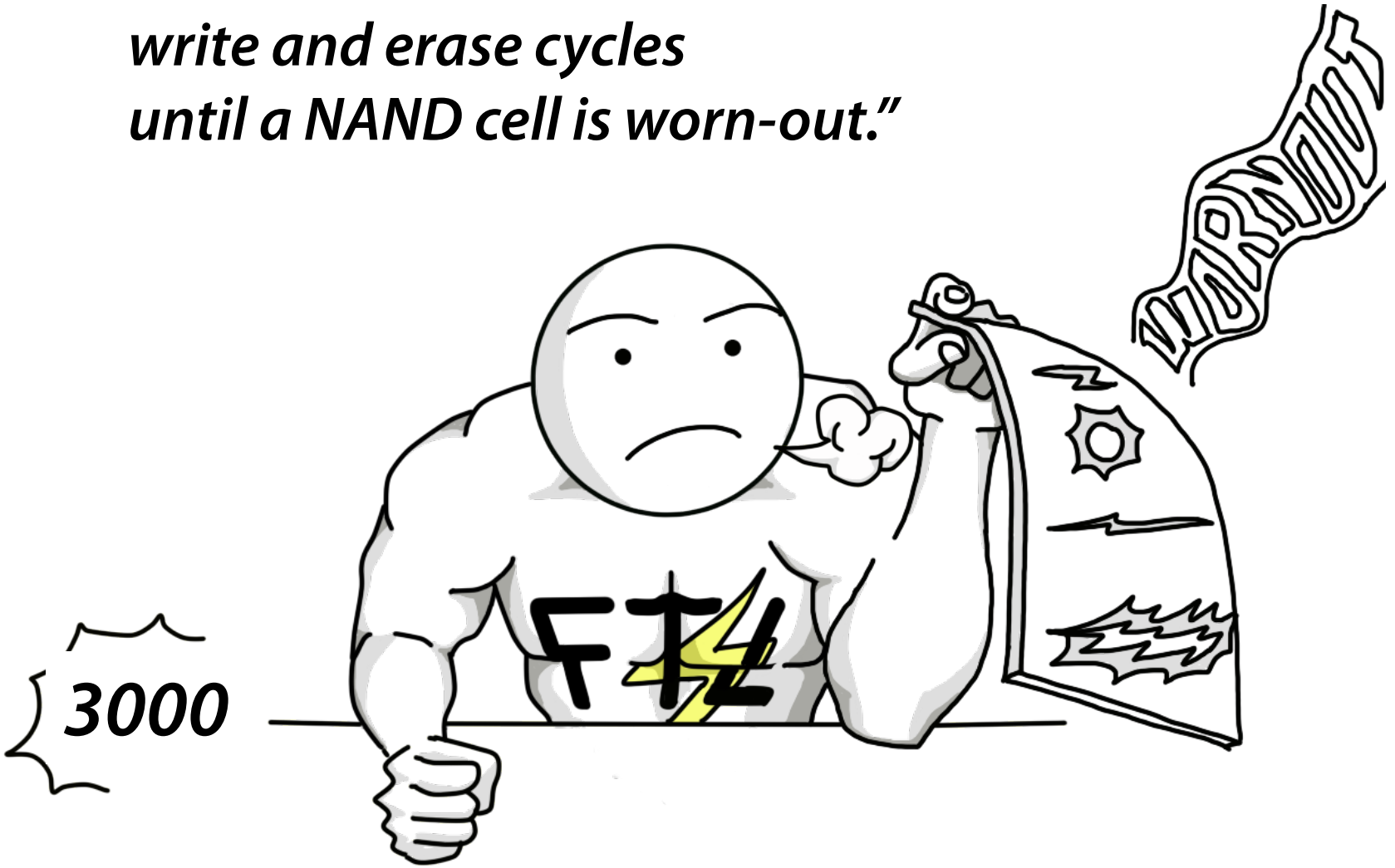
Trend of NAND Device Technologies



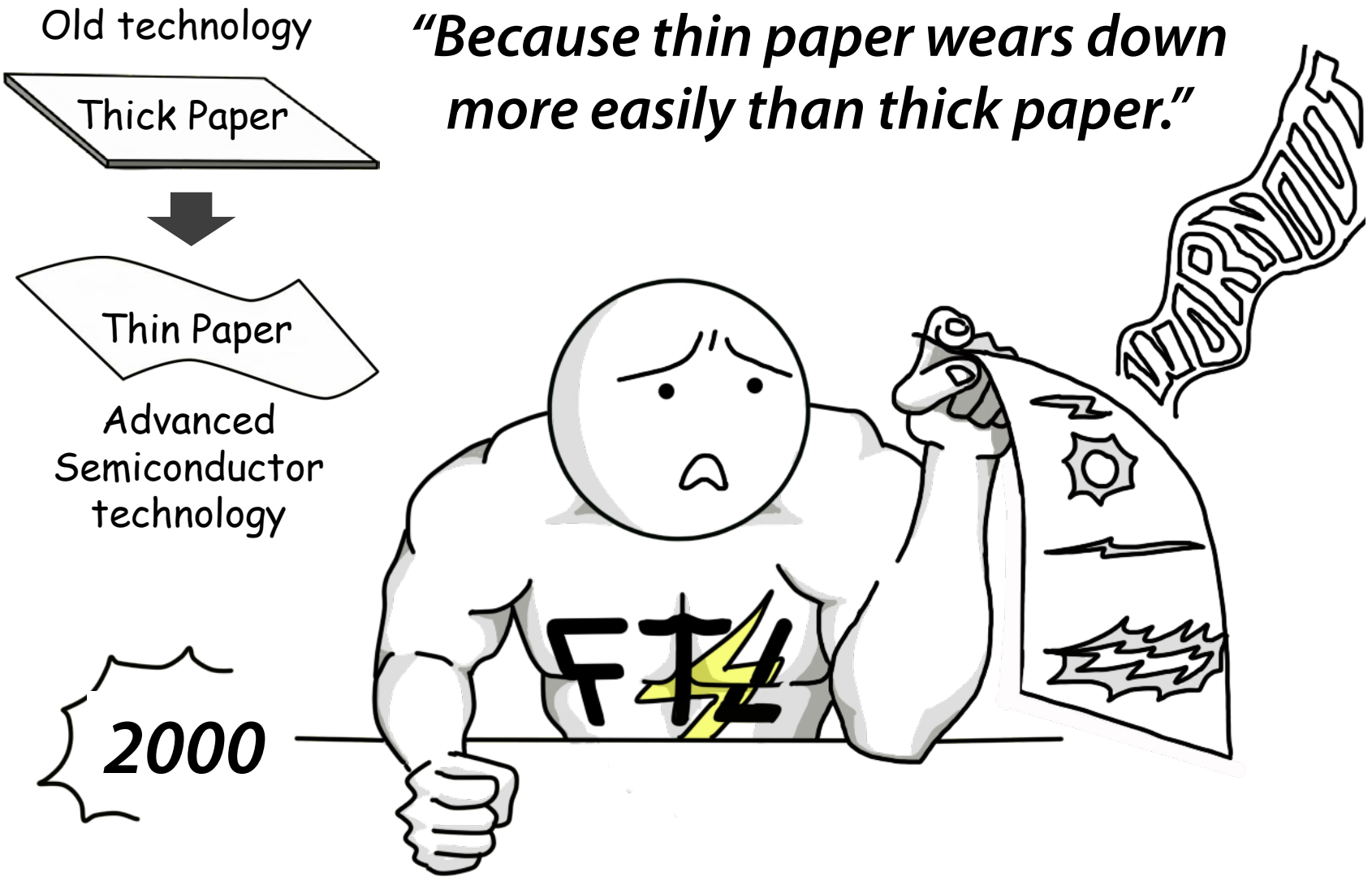
But, NAND endurance is drastically decreased last 6 years.

What is the NAND Endurance ?

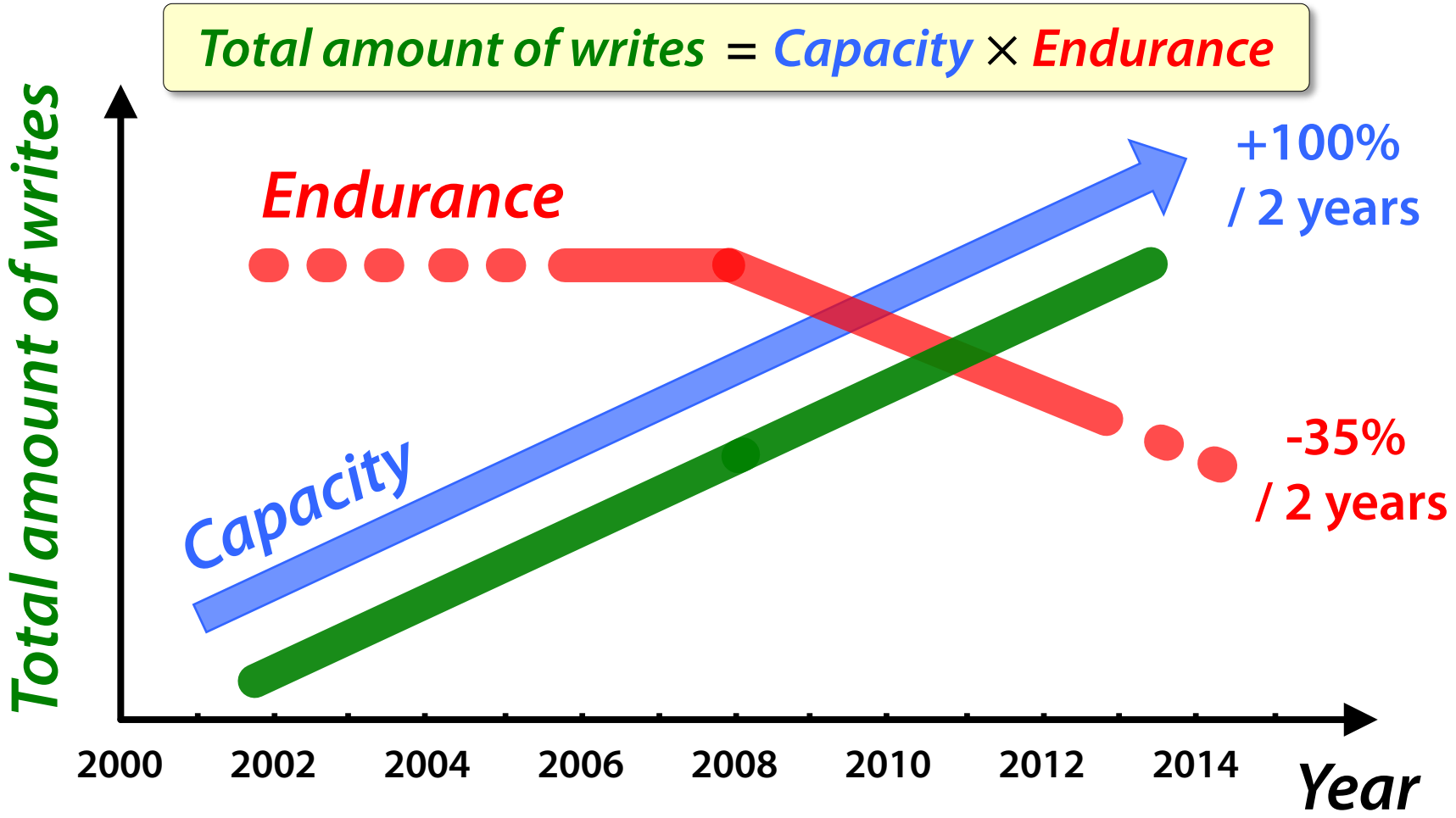
"The maximum number of write and erase cycles until a NAND cell is worn-out."



Why is the NAND Endurance Decreased ?



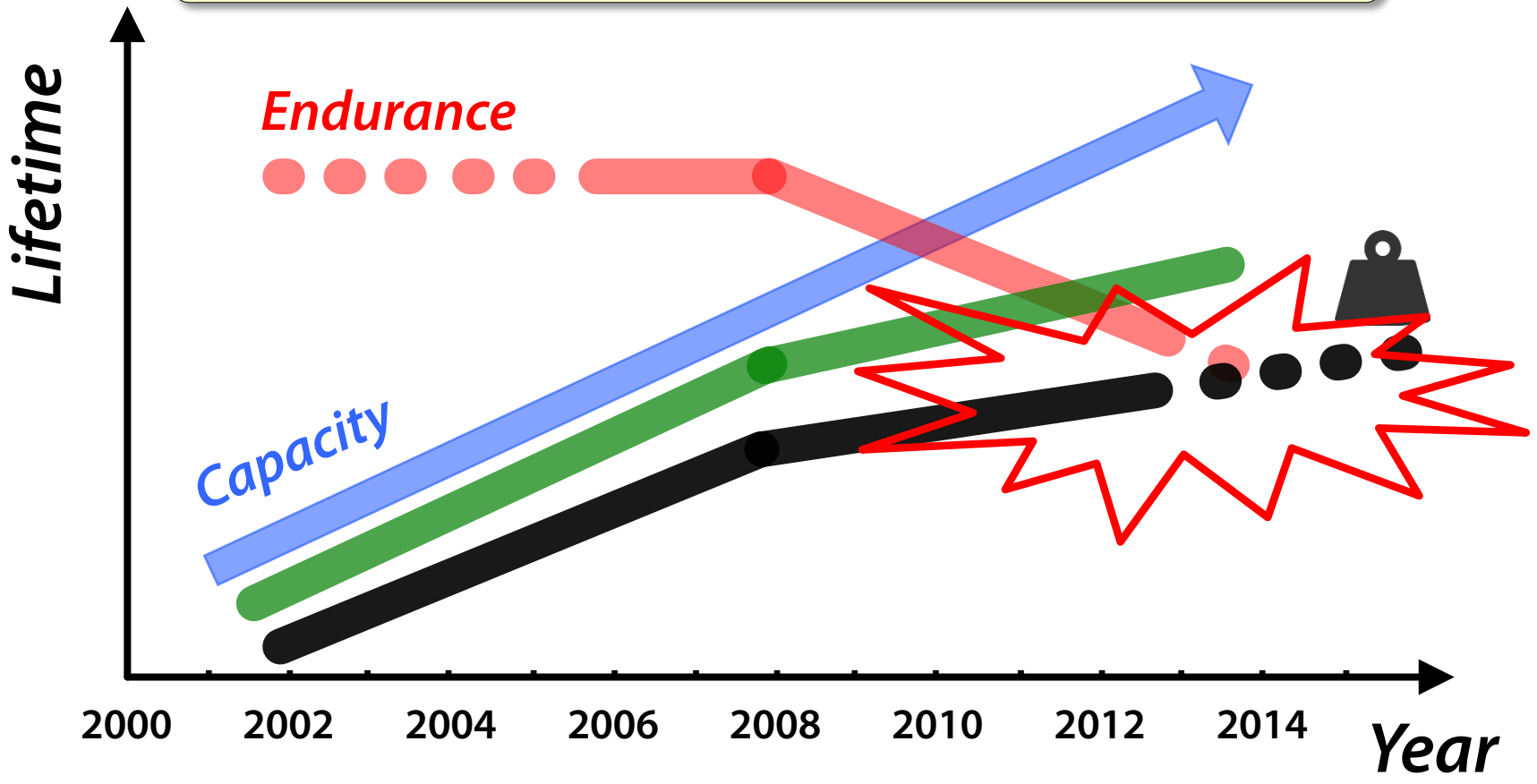
Trend of NAND Device Technologies



Total amount of writes of NAND flash-based storages does not increase as much as we expected.

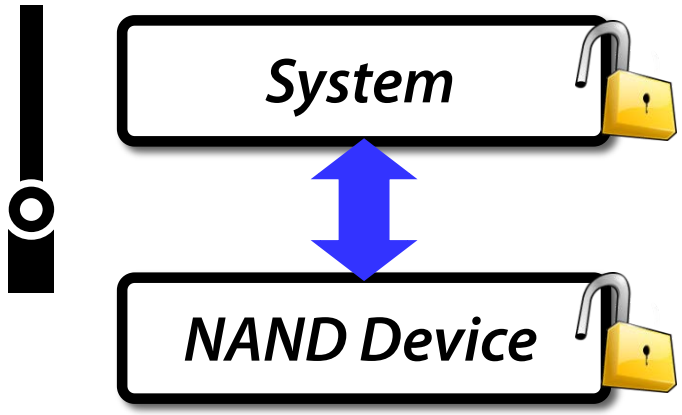
Lifetime Problem of NAND-based Storages

$$Lifetime = \frac{Total\ amount\ of\ writes}{Daily\ amount\ of\ data}$$



Decreasing lifetime is a main barrier for sustainable growth.

Previous Research for Improving Lifetime



Our goal



$$\textit{Lifetime} \propto \frac{\textit{Capacity} \times \textit{Endurance}}{\textit{Daily workload} \times \textit{WAF}}$$

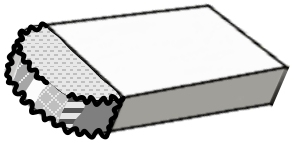
- *Daily workload*
  - *Deduplication*
  - *Compression*
  - *Throttling*
- *WAF*
  - *Optimization of garbage collection & wear leveling*

Key Idea to Improve the NAND Endurance

(1) Erasing with a lower erase voltage

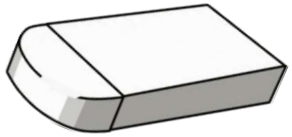
(2) Slowly erasing

Hard Eraser



High Erase Voltage

Soft Eraser

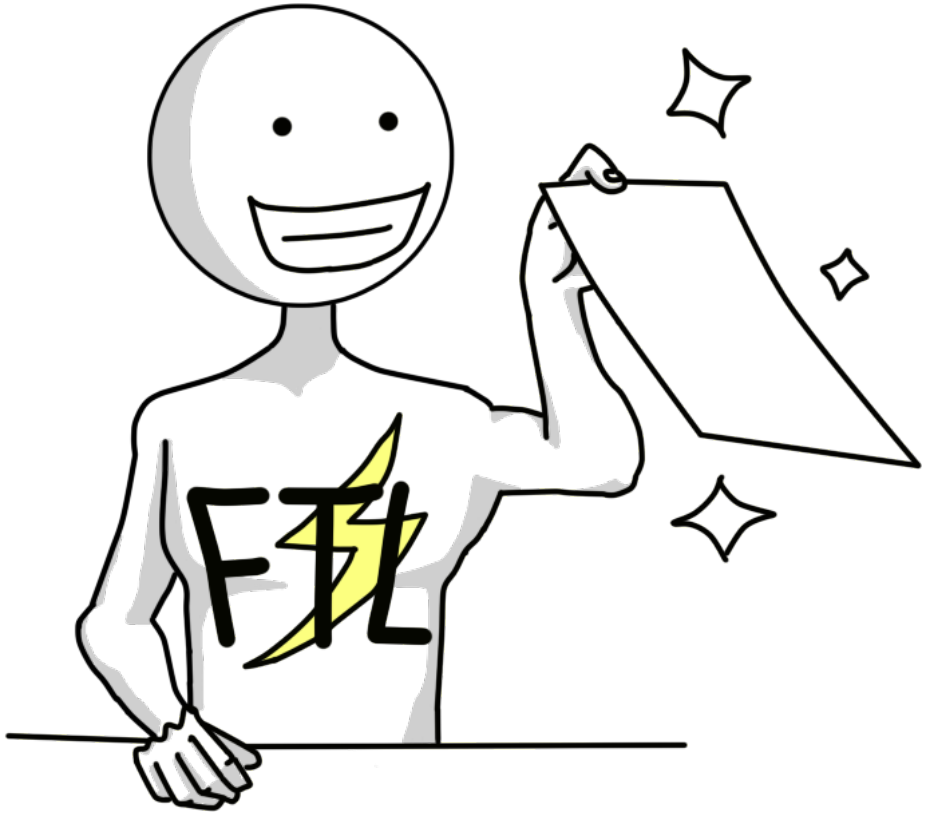


Low Erase Voltage



"2000"

4000



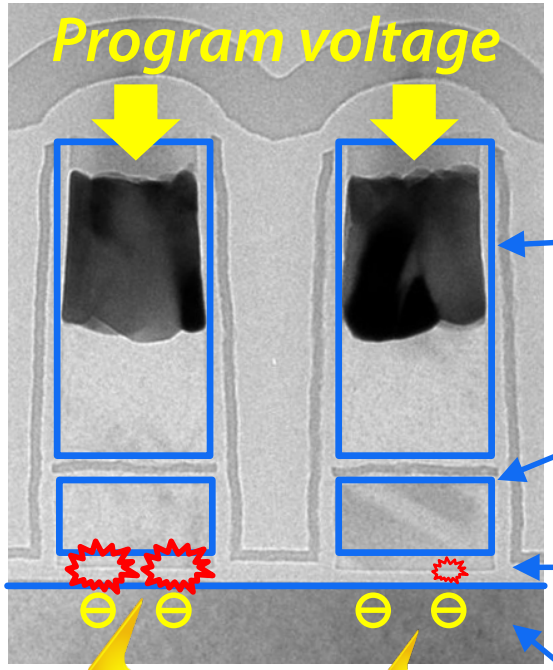
Motivation : Device Physics Model

Fast erase with a high erase voltage

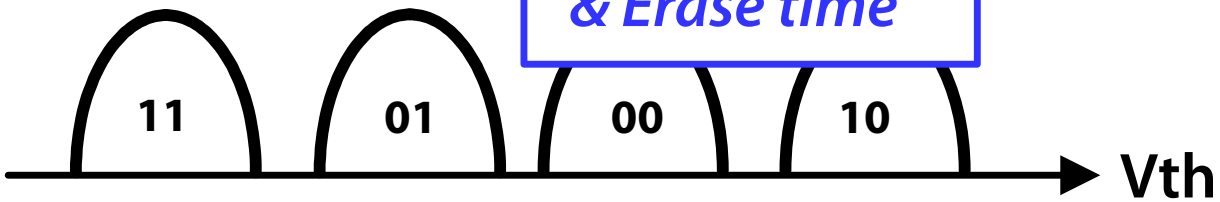


High damage

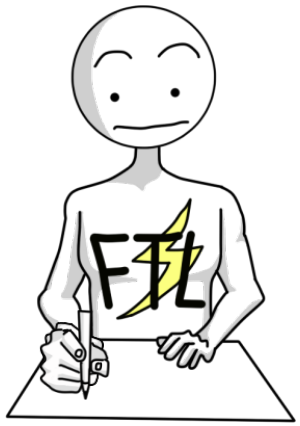
Cross-section view of NAND flash memory cells



Erase voltage & Erase time



Slow erase with a lower erase voltage



Low damage

Overview of Our Proposed Approach

DPES (Dynamic Program and Erase Scaling) approach

Erase Voltage Scaling	*Erase Time Scaling*	*Program Time Scaling*
Endurance vs. Erase Voltage	*Endurance vs. Erase Time*	*Erase Voltage vs. Program Time*



Dynamically changes **program** and **erase voltage/time



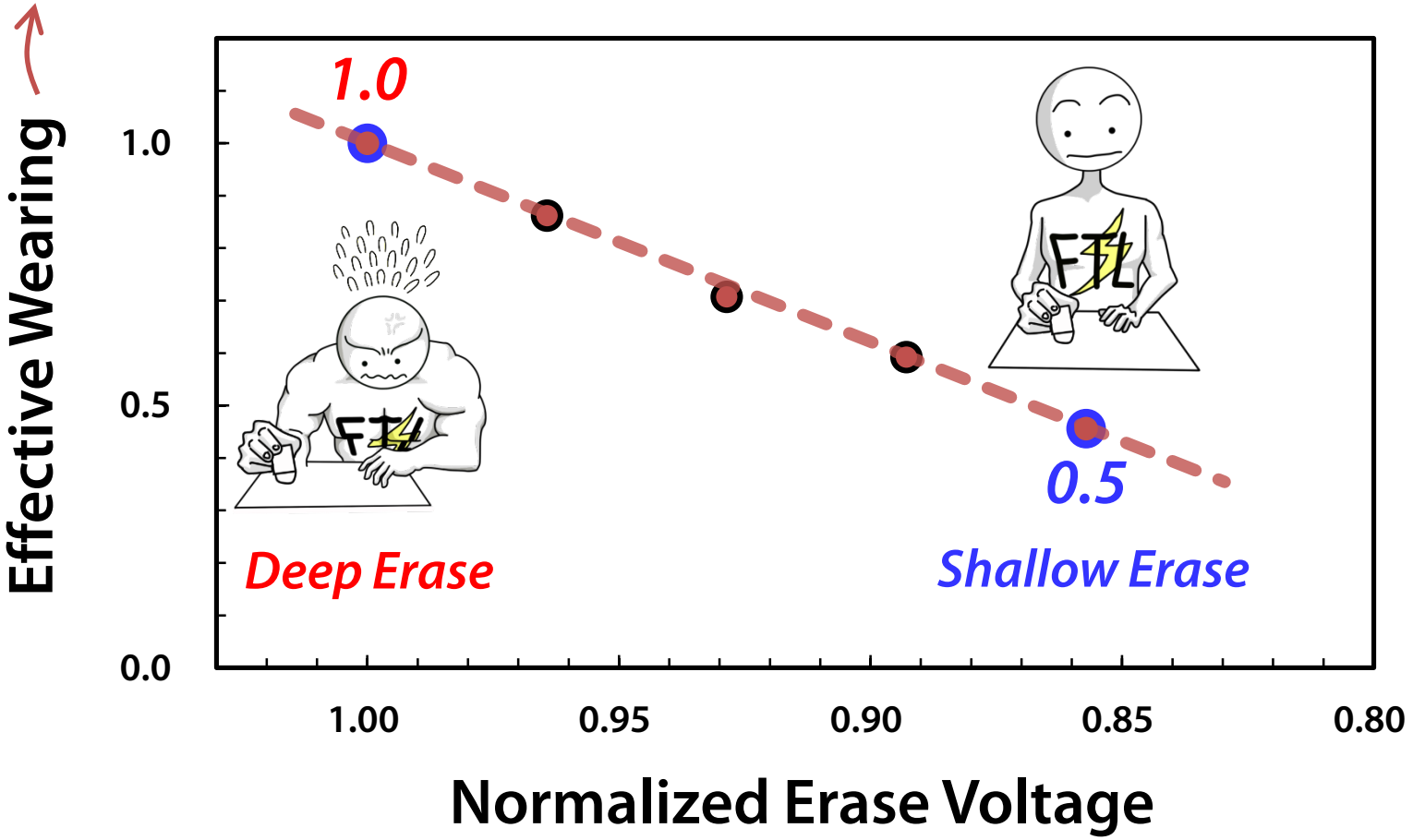
Improves the NAND **endurance
w/o degradation in the overall write **throughput

Outline

- Lifetime Issues in NAND Flash-based Storages
- **Key Components of the DPES Approach**
- Implementation of DPES-aware FTL
- Experimental Results
- Conclusions
- Q & A

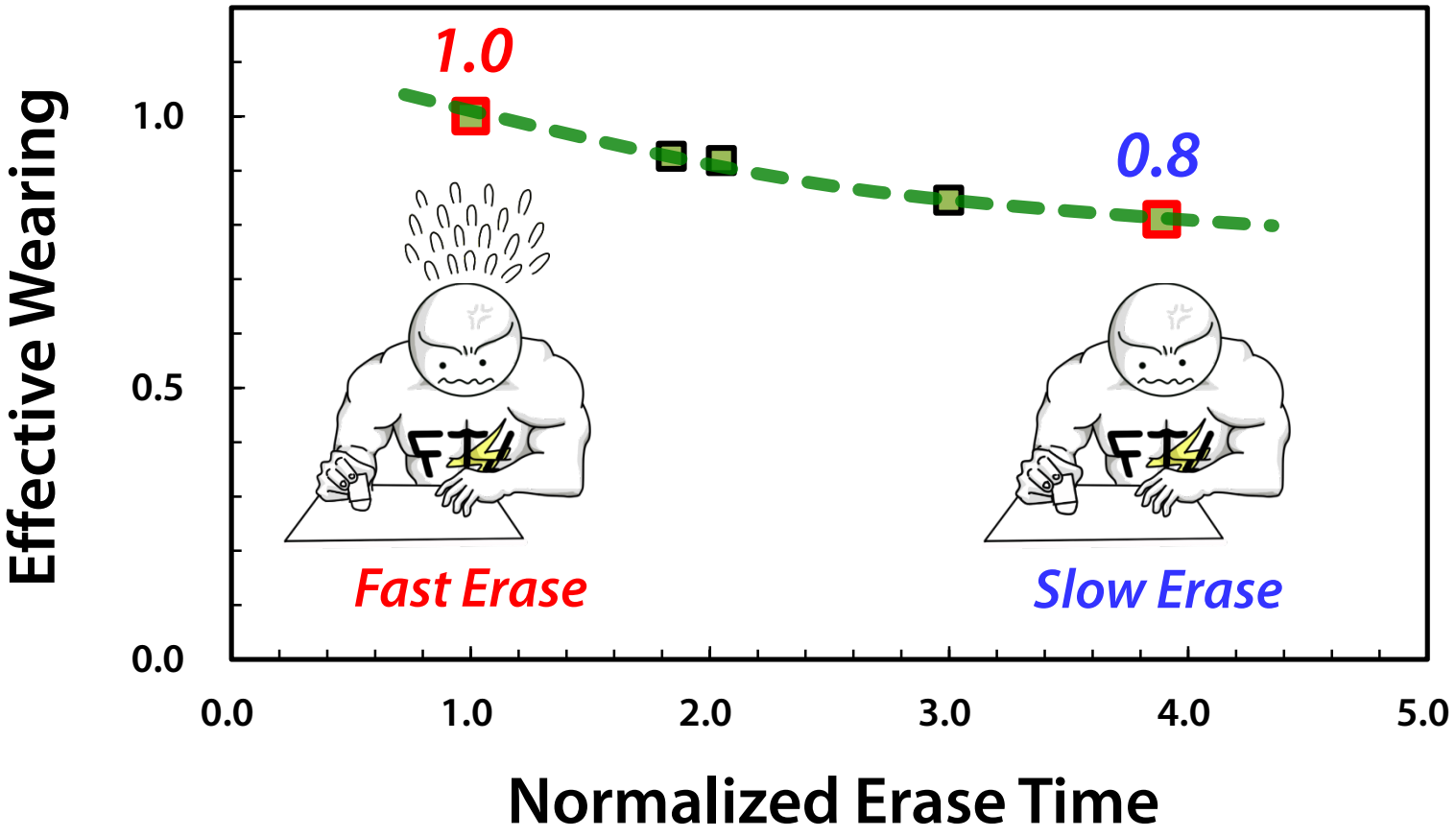
Erase Voltage Scaling

"The effective degree of NAND damage after one P/E cycle."



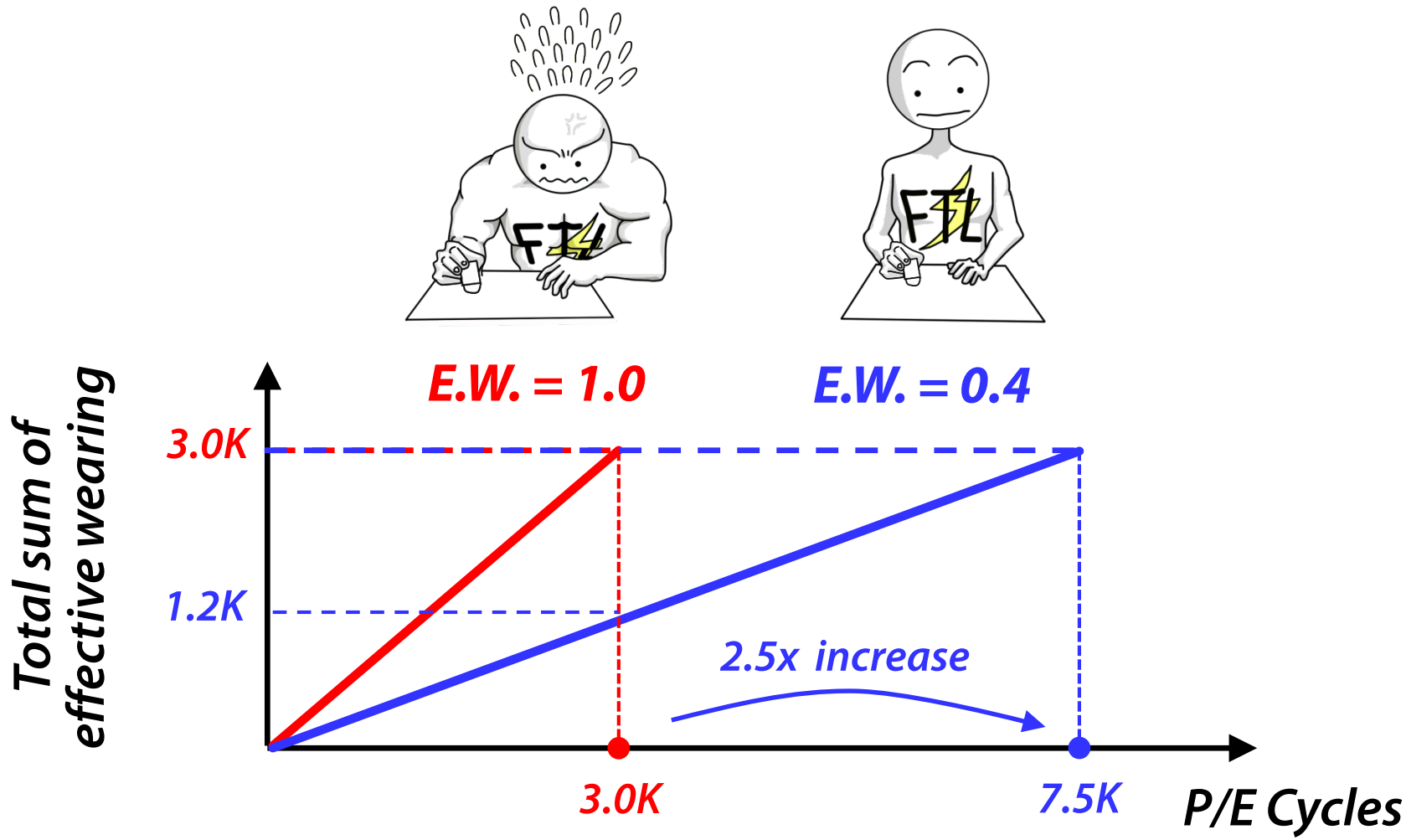
Lowering an erase voltage can reduce the effective wearing.

Erase Time Scaling

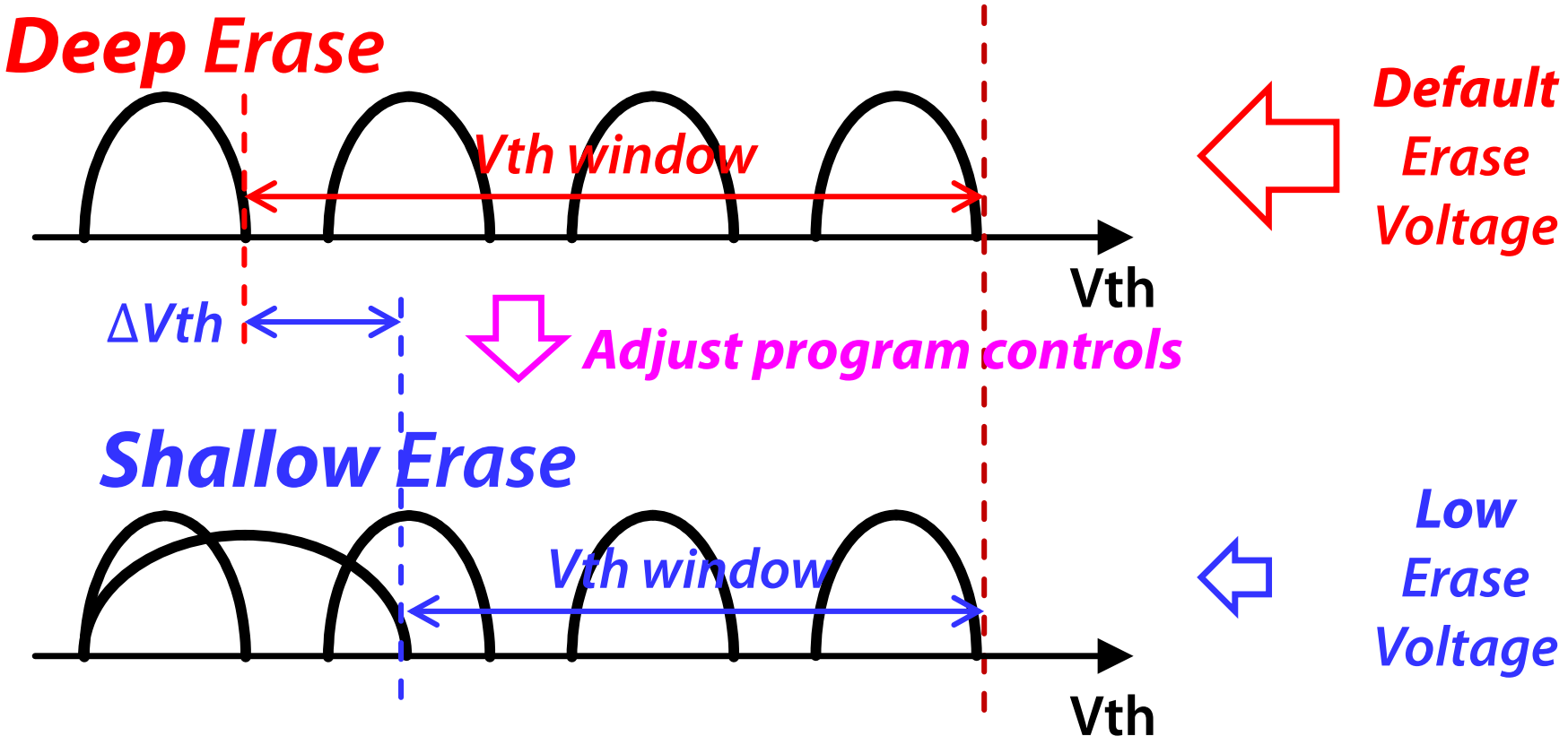


Slowly erasing can further reduce the effective wearing.

Effect of Erase Voltage/Time Scaling

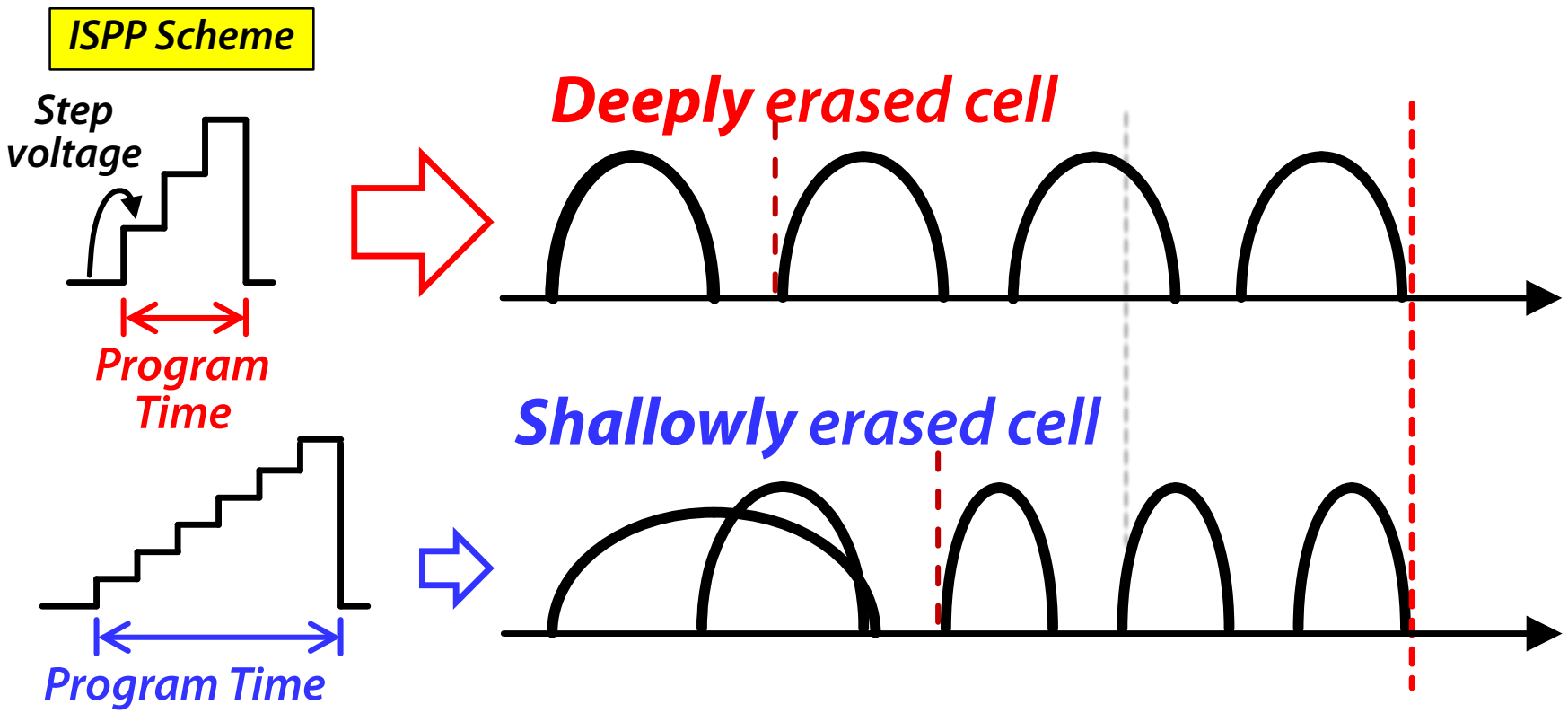


Side Effect of Erase Voltage Scaling



When a low erase voltage is used, Vth distributions should be formed within the narrow Vth window.

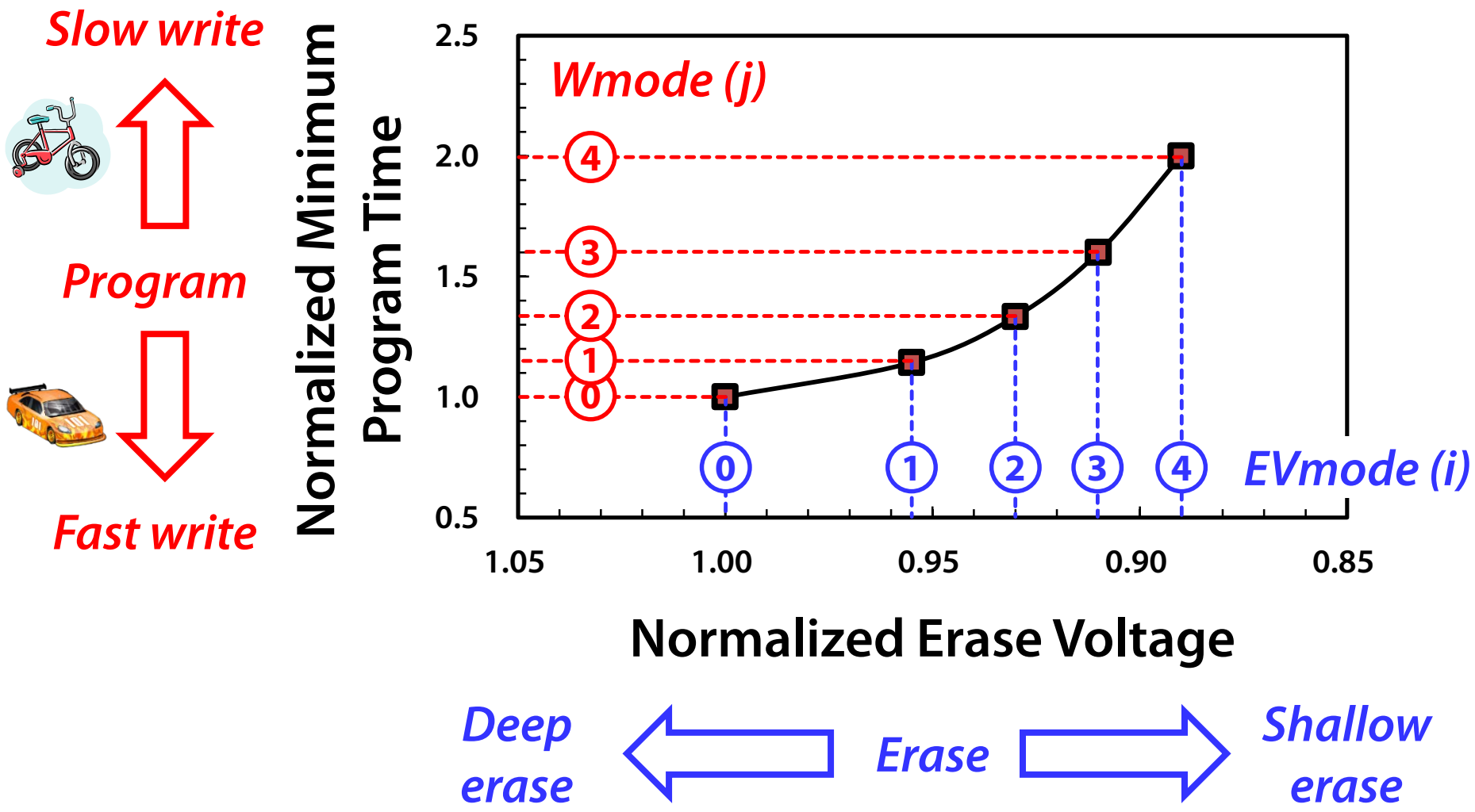
Program Time Scaling



To form narrow Vth distributions, the program time is increased.

Program controls should be differently adjusted for blocks erased with different erase voltages.

Tradeoff : Erase Voltage vs. Program Time



Dynamic Program and Erase Scaling



High erase voltage
Fast erase speed

Dynamic Program & Erase Scaling

Low erase voltage
Slow erase speed

Low Endurance
High Performance

High Performance
High Endurance

High Endurance
Low Performance

Erase voltage	Wearing	Minimum program time
High	High	Short
• • •		
Low	Low	Long

DPES-Enabled

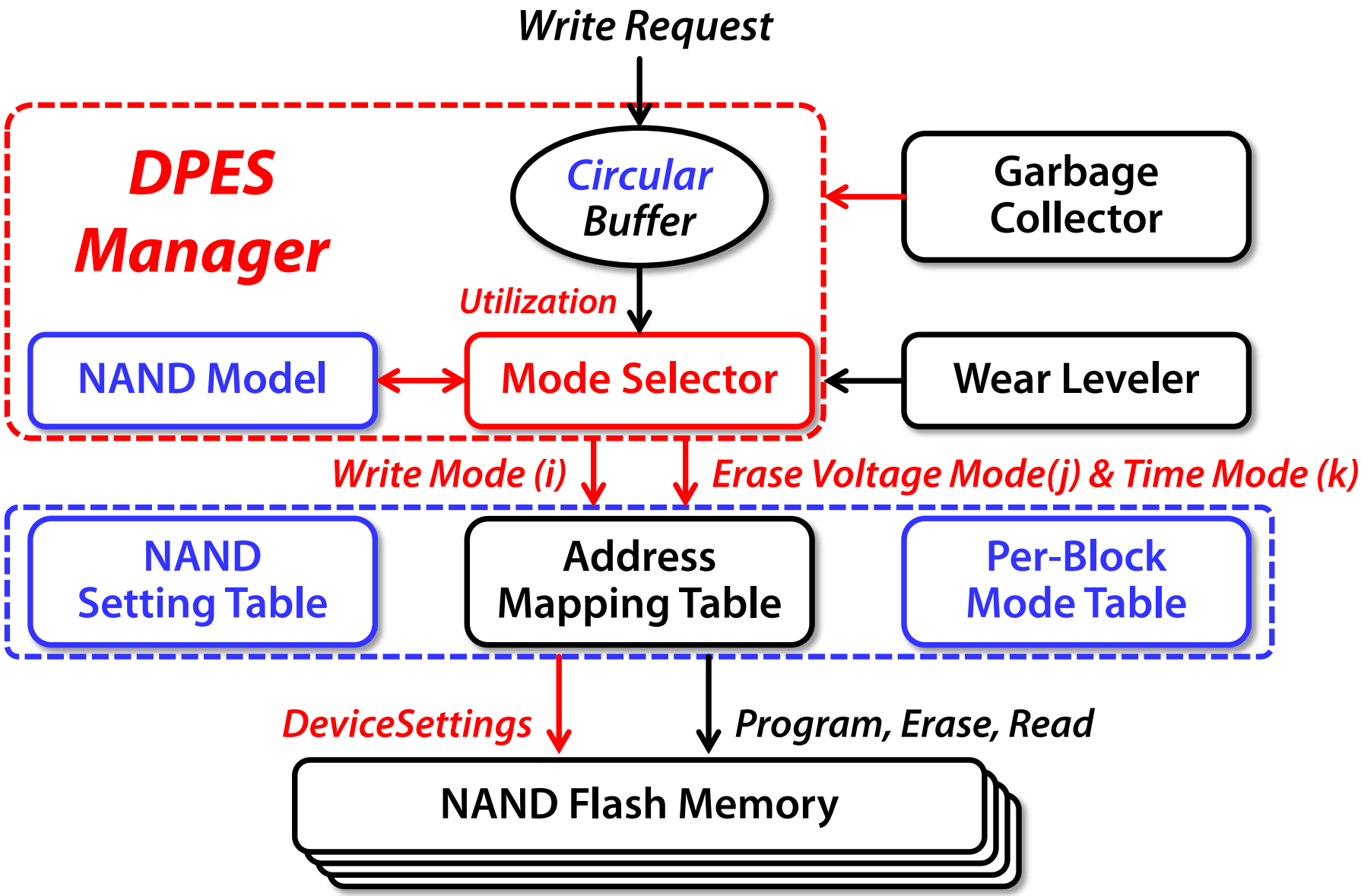
NAND Chip

Erase speed	Wearing
Fast	High
Slow	Low

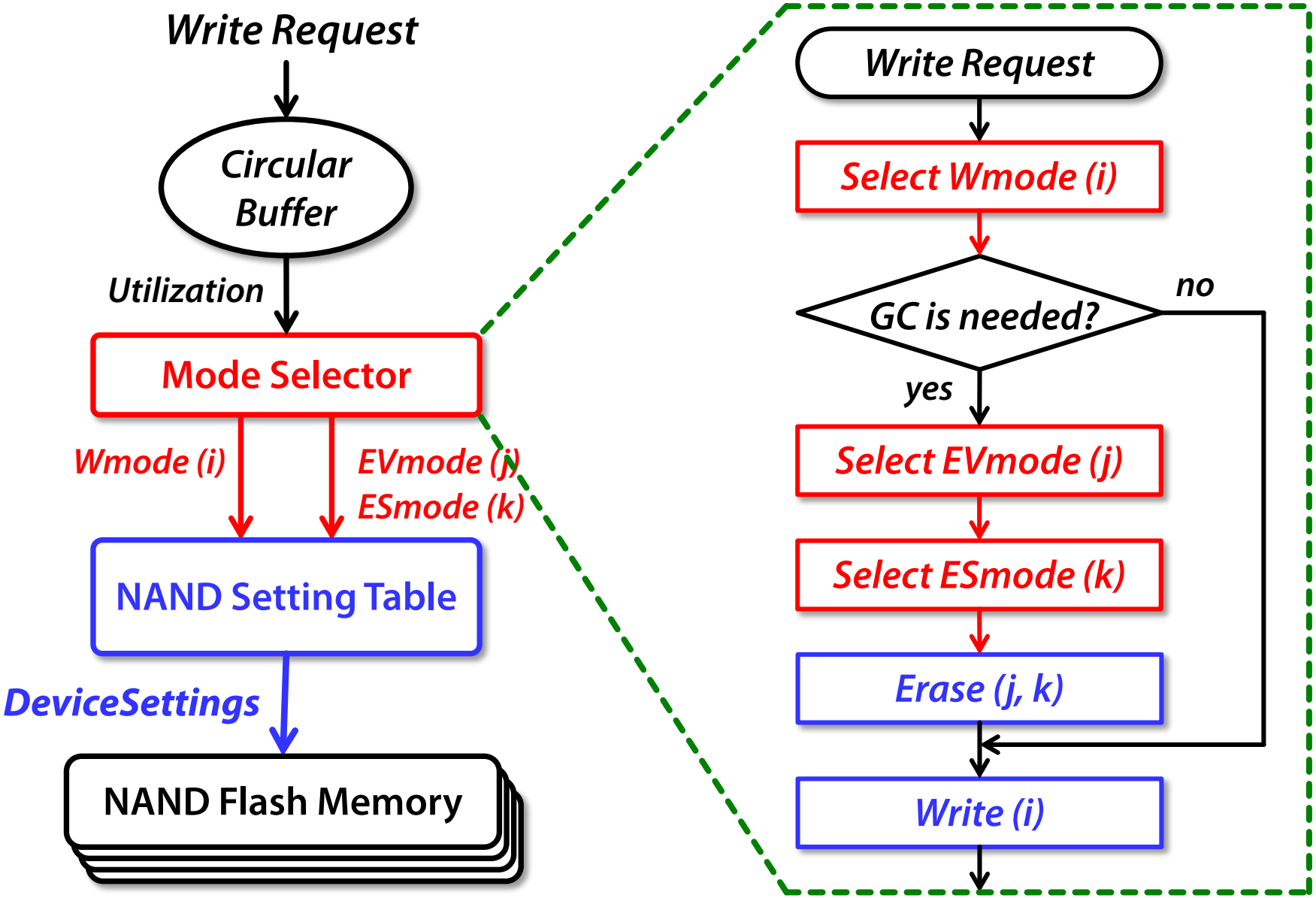
Outline

- Lifetime Issues in NAND Flash-based Storages
- Key Components of the DPES Approach
- **Implementation of DPES-aware FTL**
- Experimental Results
- Conclusions
- Q & A

Overview of DPES-enabled FTL *(AutoFTL)*

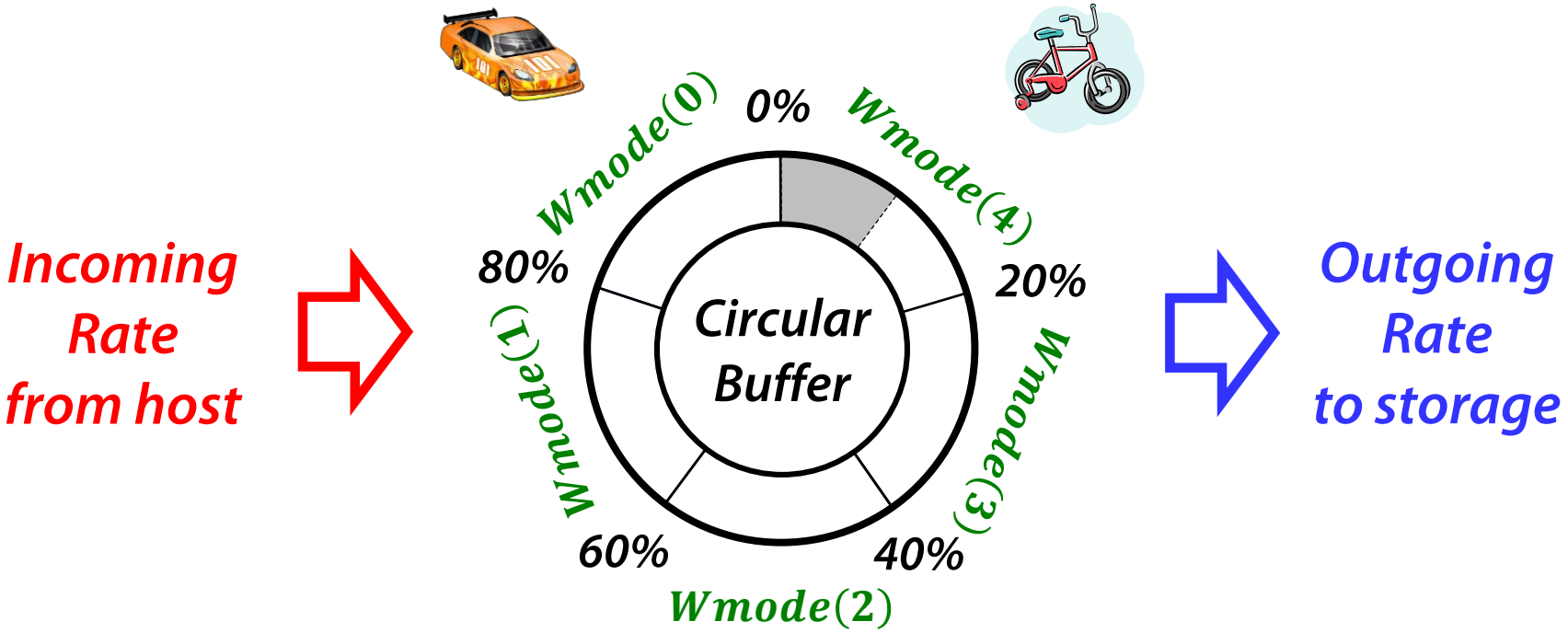


Write & Erase Modes Selection Flow



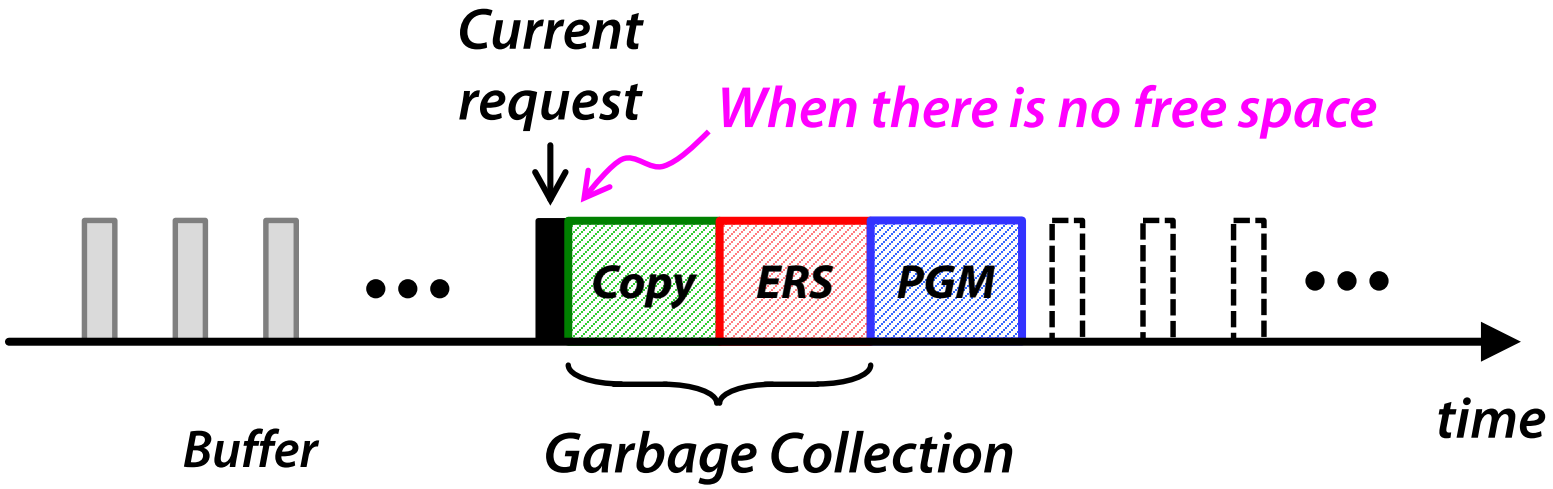
Write Mode Selection

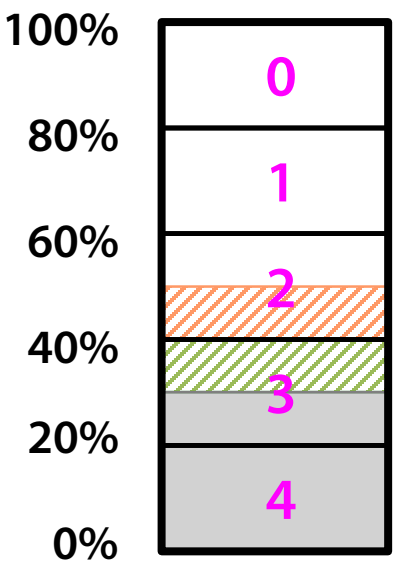
- AutoFTL uses a ***circular buffer*** for deciding the most appropriate write mode.



Buffer utilization is increased !!
Buffer utilization is decreased !!

Erase Voltage Mode (EV_{MODE}) Selection





Without G.C. : $u = 30\%$ → $Wmode(3)$

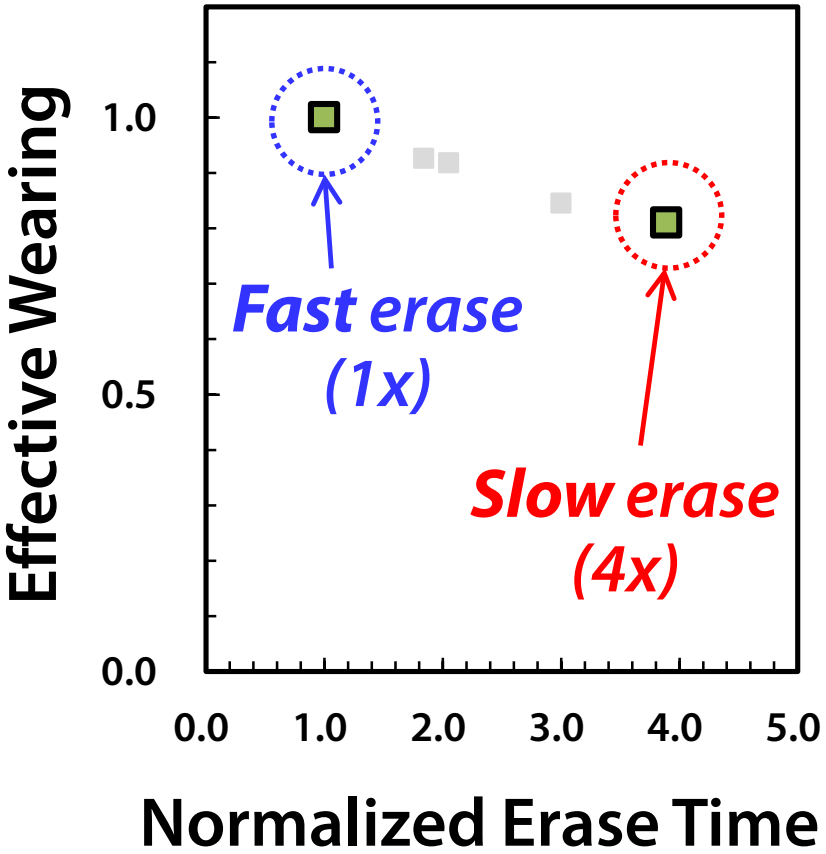
With G.C. : $u^* = u + \Delta u^{copy} + \Delta u^{erase}$

$= 30\% + 10\% + 10\% = 50\%$

→ $Wmode(2)$ → $EVmode(2)$

Erase Speed Mode (ES_{MODE}) Selection

$$u^* = u + \Delta u^{erase} = u + \frac{EraseTime}{ProgramTime} \times \frac{1}{Nr_Entry} < 100\%$$

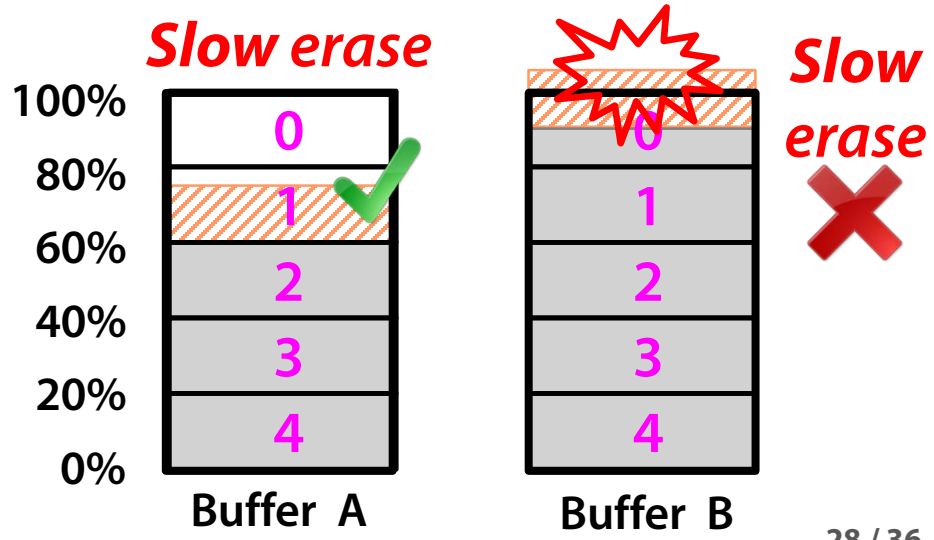


(Example)

- *100-entries buffer*
- *Operation time*
  - *Program: 1.3 ms*
  - *Fast erase: 5 ms*

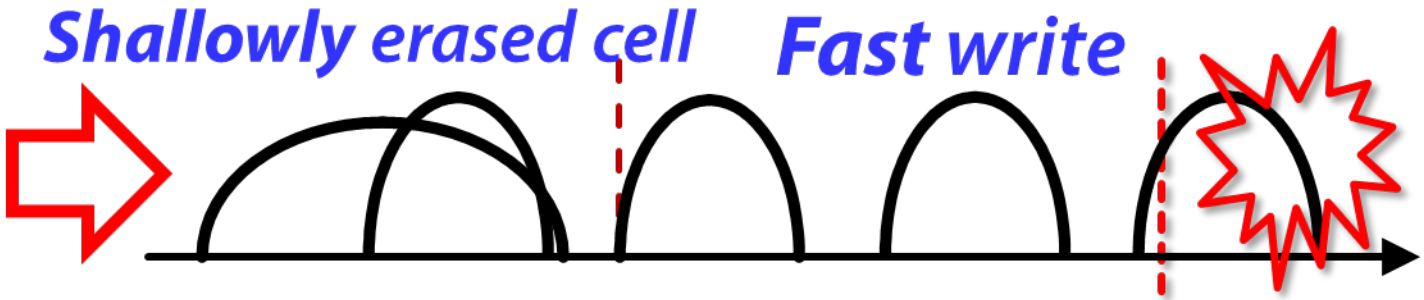
$\Delta u^{fast\text{-}erase} = 3.8\%$

$\Delta u^{slow\text{-}erase} = 15.2\%$

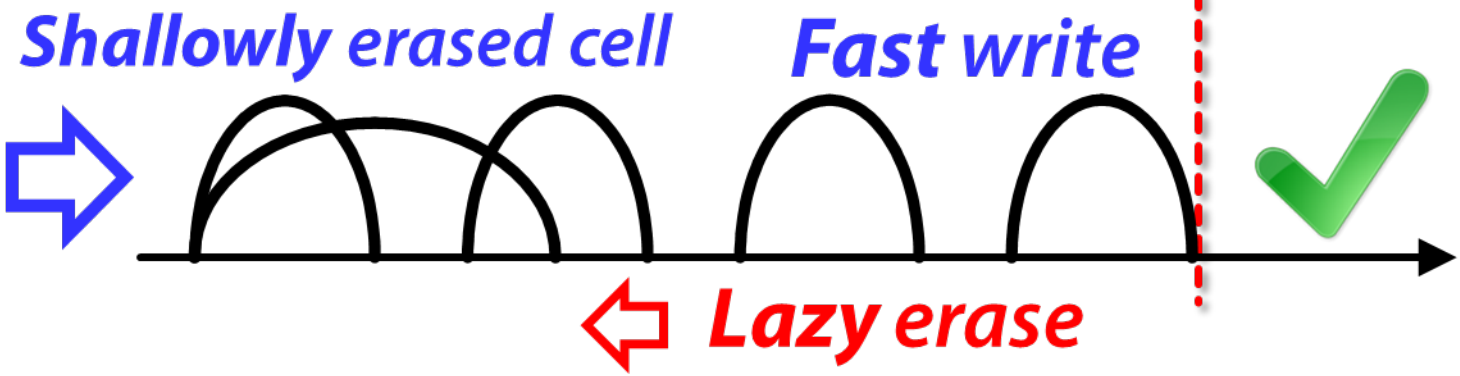


Mismatch: Erase Mode vs. Write Mode

Write request → Fast write mode is selected. → But, there are only shallowly erased blocks.



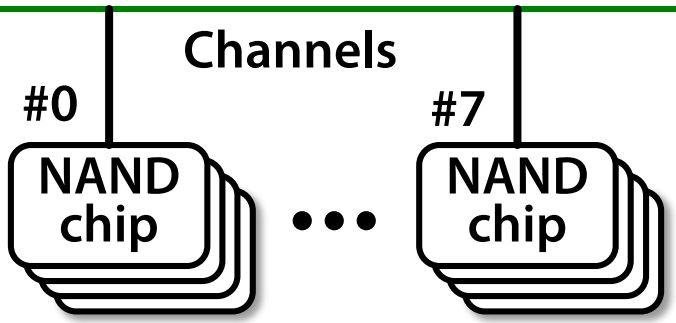
How to use fast write mode for a shallowly erased block ?



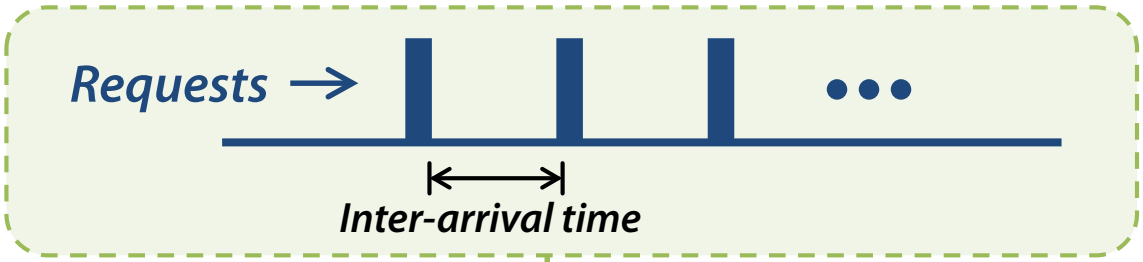
Outline

- Lifetime Issues in NAND Flash-based Storages
- Key Components of the DPES Approach
- Implementation of DPES-aware FTL
- **Experimental Results**
- **Conclusions**
- Q & A

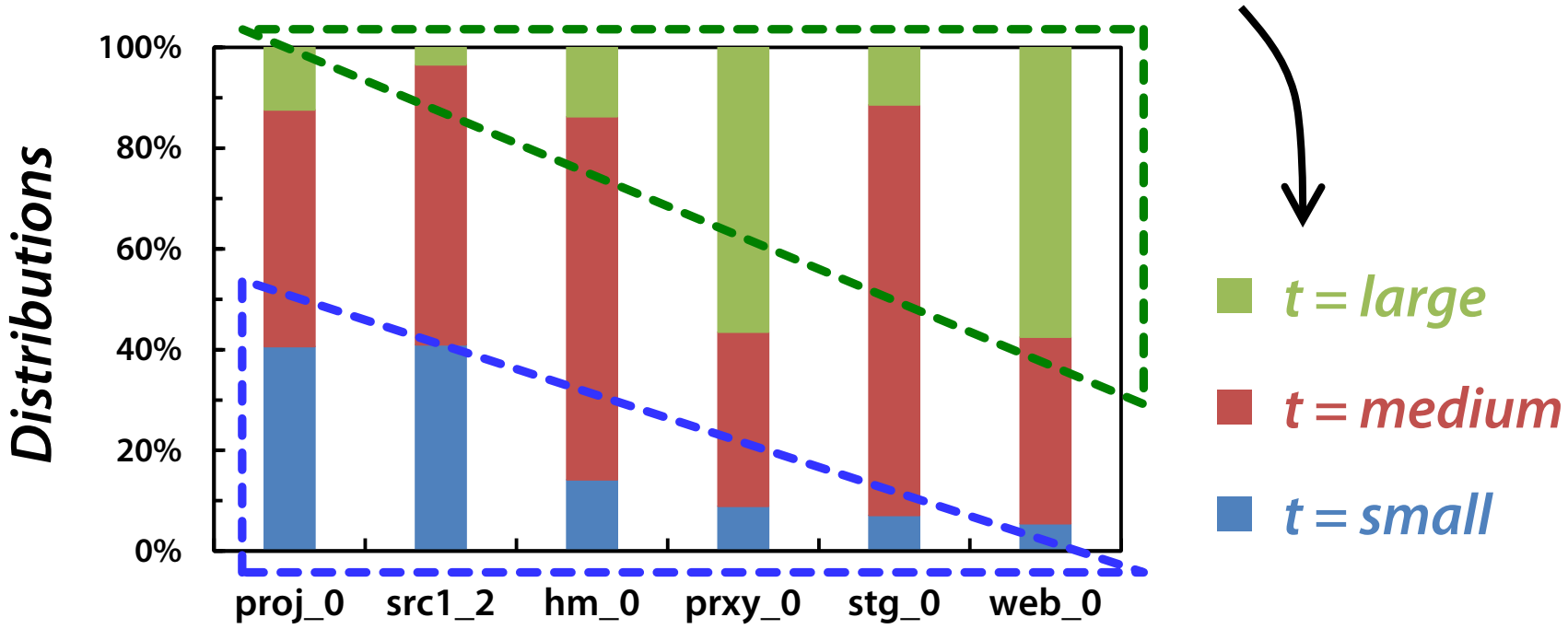
Experimental Settings

Write Request	6 enterprise traces from MSR Cambridge	
Buffer Size	32 MB (= 4096 entries × 8 KB)	
NAND Model	Write mode	0, 1, 2, 3, 4
	Erase voltage mode	0, 1, 2, 3, 4
	Erase speed mode	Fast, slow
NAND Configurations		

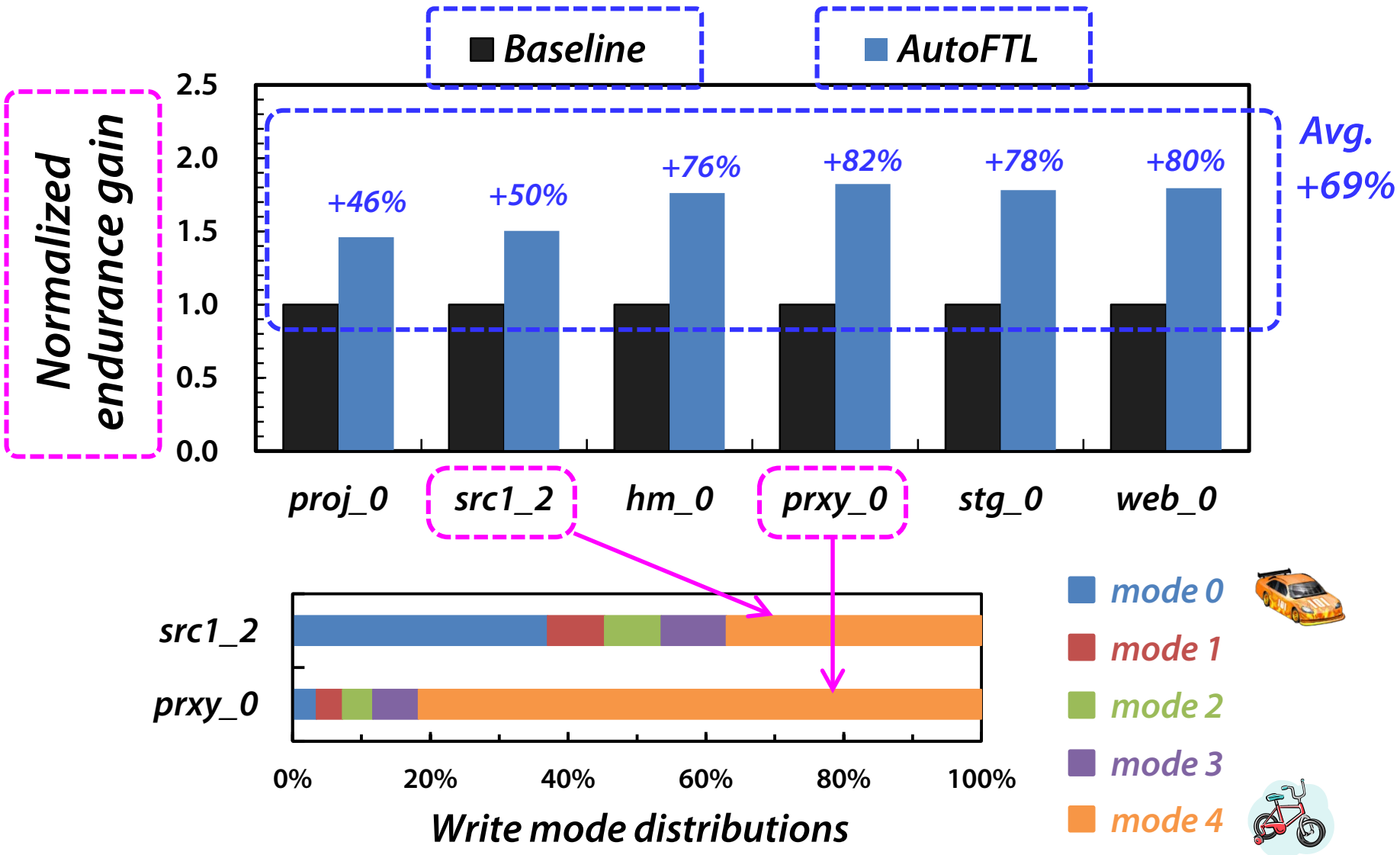
Characteristics of I/O Traces



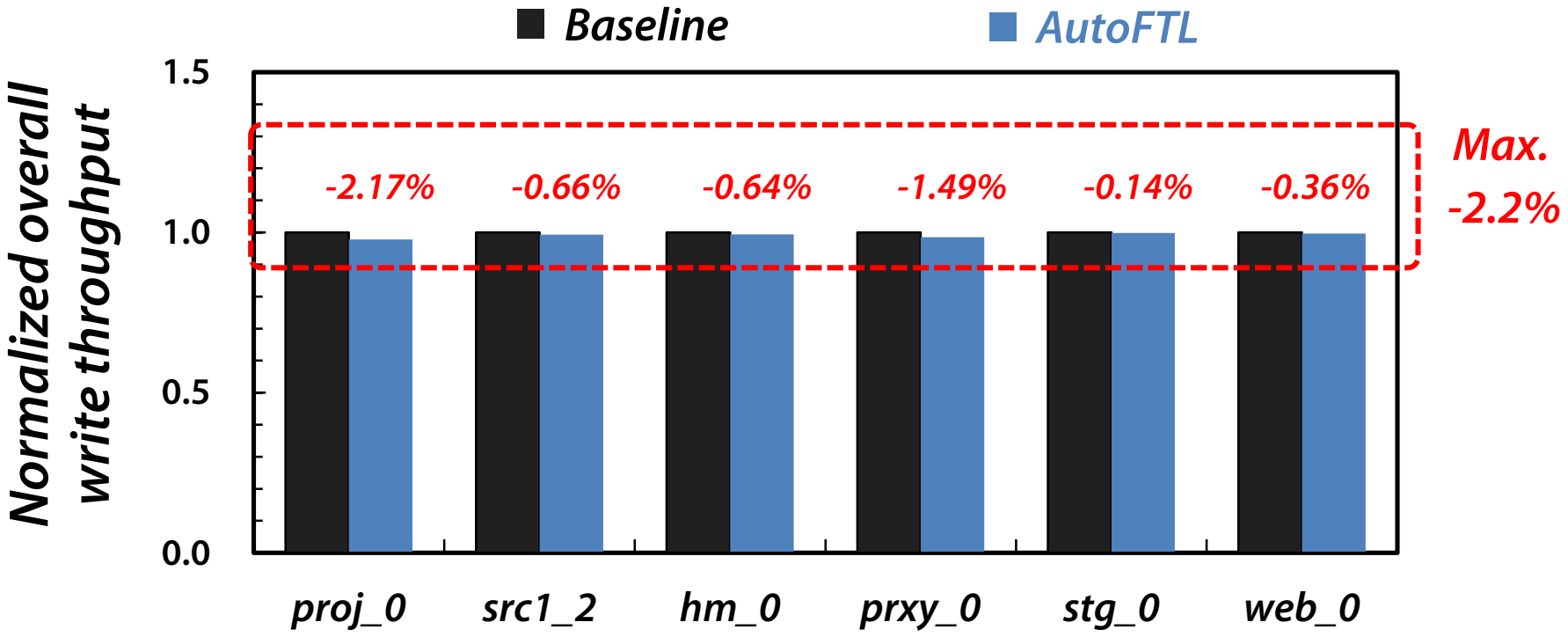
Distributions of normalized inter-arrival times (t)



Overall Endurance Gain

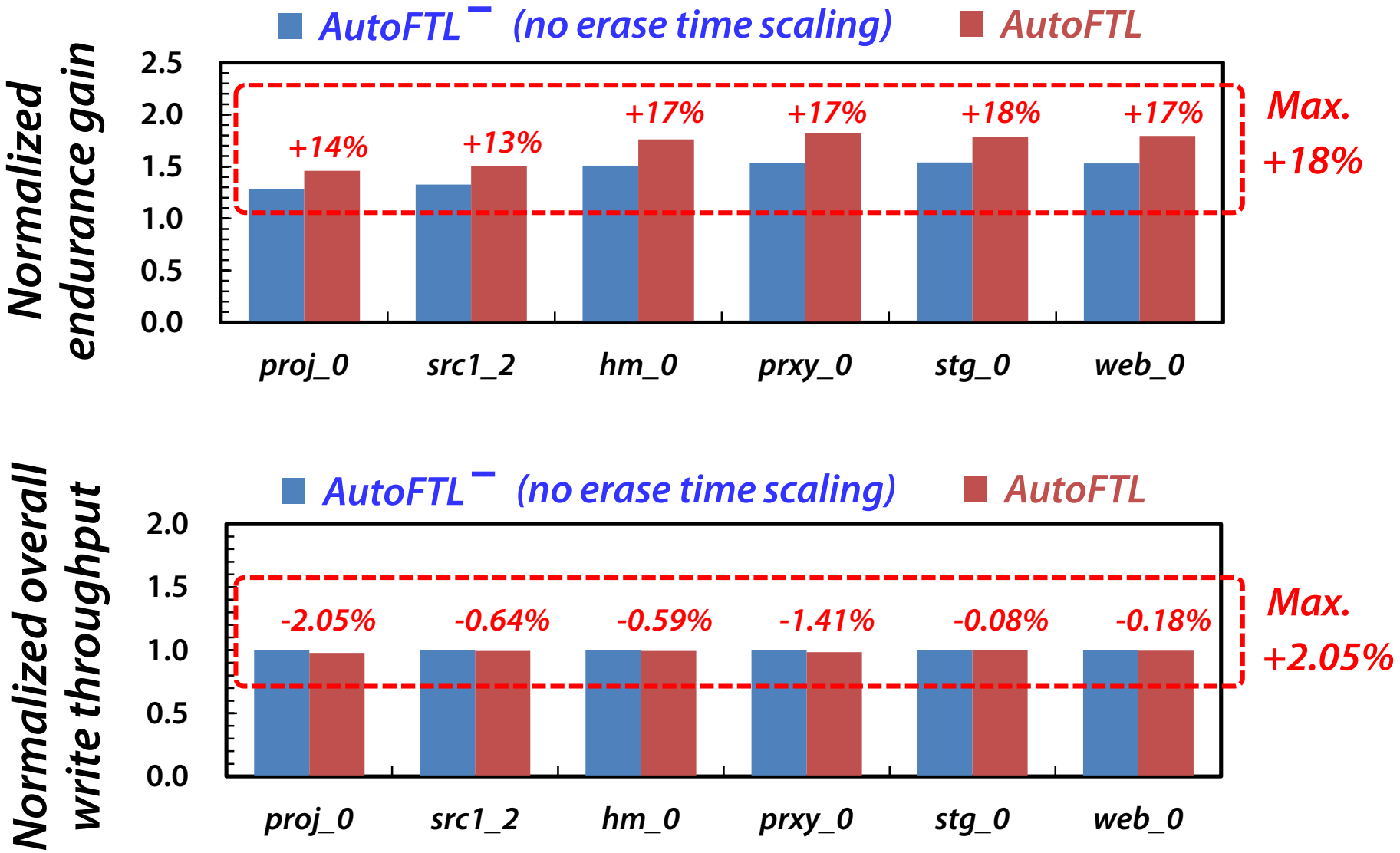


Overall Write Throughput



- ✓ *The overall write throughput degradation was less than 2.2%.*
- ✓ *Lazy erases were very rare: less than one lazy erase per 1000 erases.*

Effect of Erase Time Scaling



Conclusions

- ✓ **We have presented the *DPES approach* for improving the lifetime of flash-based storage systems**
  - ***Actively exploits the tradeoff relationship between the NAND endurance and the erase voltage/time.***
  - ***Implemented the DPES-aware FTL (autoFTL) which dynamically changes multiple erase and write modes.***
- ✓ **The NAND endurance was improved by 69% on average with less than 2.2% decrease in the overall write throughput.**